EKT422 - Computer Architecture

This course is *Computer Architecture*, offered by the School of Computer and Communication Engineering.

Academic Session 2010/2011

This semester (semester 1), I will be handling this course for students in the Computer Engineering and Communication Engineering programs.

Announcement

[**20101022**] Mini Project 2 Report due at 12pm on Oct 1, 2010. Email a softcopy AND pass the hardcopy to me!

[**20100902**] Happy Eid to all my Muslim students! To everybody else, have fun. I'll see you guys after the break.

[**20100829**] We will have a tutorial session during lab-hours this week (30/08/2010). This will most probably be conducted by En. Muslim.

[**20100820**] Test 1 will be held on Aug 21 @Automart Complex (10am-11am). Please be there at least 10 minutes before time.

[**20100812**] Test 1 that was previously scheduled on Aug 14 is **POSTPONED** to Aug 21.

[**20100715**] Lab for group 4 (previously scheduled at 1700-1900) is now shifted to the 1300-1500 slot.

[**20100712**] The lab sessions for this first week is canceled. I need to adjust the schedule and it has not been finalized.

Course Assessment

The assessment components are shown below.

	Examinations			**Course Work**			
Total Contribution	70%			30%			
Assessment	Mid-Term Test	Second Test	Final Exam	Quiz/Assignments	Class Participation	Mini Project 1	Mini Project 2
Contribution	10%	10%	50%	5%	5%	10%	10%

[Update20100825] The assessment components has been reviewed. Notice that only the course

component has been modified. So, Final Exams will only cover chapters 1-15. Chapters 16-18, if time permits, will be assessed in the special test.

	Examinations			**Course Work**				
Total Contribution	70%			30%				
Assessment	Mid-Term Test	Second Test	Final Exam	Quiz/Assignments	Class Participation	Mini Project 1	Mini Project 2	Special Test
Contribution	10%	10%	50%	5%	5%	5%	5%	10%

[Update20101116] The assessment components has been reviewed (AGAIN) as follows. This is FINAL.

	Examinations			**Course Work**			
Total Contribution	70%			30%			
Assessment	Mid-Term Test	Second Test	Final Exam	Quiz/Assignments	Class Participation	Mini Project 1	Mini Project 2
Contribution	10%	10%	50%	10%	5%	5%	10%

Course Outcome

I slightly modified the course outcome so that it'll become more clear and concise (at least from MY point of view).

1. **[CO1]** able to explain the theoretical aspects of computer organization and architecture
2. **[CO2]** able to analyze design issues involving cost and performance
3. **[CO3]** able to design basic CPU based on given specifications

For reference, here are the original COs:

1. **[CO1]** Understand the theory and the architecture of a central processing unit
2. **[CO2]** Ability to analyze some design issues in term of speed, technology, cost and performance
3. **[CO3]** Ability to design a simple CPU with applying the theory and knowledge in the lecture
4. **[CO4]** Ability to use appropriate CAD tool to design verify and test the CPU architecture
5. **[CO5]** Students will exercise the theoretical aspects in completing the lab works and lab test

Notice that some of the old outcomes are redundant and I feel the COs I have defined basically covers all aspect of the previous COs except for CO4. I purposely leave this one out because I think the CAD tools that we have are not specific for testing and verification of CPU architecture. The tools being used for this course are basic digital design tools which CAN be used to test and verify ANY digital design with proper simulation models and test vectors. So, the students will STILL go through the process, but I'd rather not put that as a CO.

Update20100820: Due to my own mistakes, I am unable to officially use this new list of COs. The procedures involved in changing this turns out to be huge - need endorsements from the Senate. I can't imagine why... but, that's how it is. So, I'll re-map everything back to the old CO (will have a small problem on the lab implementation though).

Update20101223: Actually, the COs that I refer to were an older version. The one that is in the system is the first four:

1. **[CO1]** Understand the theory and the architecture of a central processing unit
2. **[CO2]** Ability to analyze some design issues in term of speed, technology, cost and performance
3. **[CO3]** Ability to design a simple CPU with applying the theory and knowledge in the lecture
4. **[CO4]** Ability to use appropriate CAD tool to design verify and test the CPU architecture

Syllabus

Week 01

- Lecture: Chapter(s) 1 - 2
- Week summary:
    1. definitions & terminology
    2. structures & functions
    3. components of computer systems
    4. history of processors (concentrate on x86 and ARM)
    5. performance measurements

Week 02

- Lecture: Chapter(s) 3 - 4
- Week summary:
    1. components of computer systems (more details)
    2. program execution, interrupts & flow control
    3. interconnections (i/o = peripherals, memory = directly addressable space)
    4. bus implementations (please read-up about PCI bus specifications, including 64-bit extension)
    5. general specifications/features of memory devices
    6. cache memory (why, how, where)
    7. cache mapping methods, replace algorithms
- ***Note**: I was not able to finish Chapter 4 - I hope to be able to squeeze it in next week's lecture*

Week 03

- Lecture: Chapter(s) 5 - 6
- Week summary:
    1. memory components and hierarchy (closest to the processor is @top)
    2. terms: ROM vs RAM vs RWM
    3. internal memory = primary memory (usu. volatile)
    4. RAM types: SRAM, DRAM, SDRAM, DDRs
    5. error correction techniques
    6. external memory = secondary memory (non-volatile, but slower)
    7. direct access? tracks, sectors and gaps (e.g. magnetic disk, optical disk)
    8. RAID disk technology
    9. sequential access: e.g. tape drive

Week 04

- Lecture: Chapter(s) 7 - 8
- Week summary:
    1. not much on chapter 8

Week 05

- Lecture: Syllabus Review

Week 06

- Lecture: Chapter(s) 9
- Week summary:
    1. integer representations (signed, unsigned)
    2. integer arithmetic
    3. floating-point representation
    4. floating-point arithmetic

Week 07

- Lecture: Chapter(s) 10 - 11
- Week summary:
    1. instruction set design
    2. addressing modes

Week 08

- Lecture: Chapter(s) 12 - 13

Week 09

- Lecture: Chapter(s) 14

Week 10

- Lecture: Syllabus Review

Week 11

- Lecture: Chapter(s) 15

Week 12

- Lecture: Chapter(s) 16

Week 13

- Lecture: Chapter(s) 17 - 18

Week 14

- Lecture: Syllabus Revision

Lab Work

- Project 1: Bus Implementation (DUE: Mid semester)
- Project 2: CPU Implementation (DUE: End of semester)

Timetable

20100712 This may be IT!

Lecture Hours

Group	Location	Day	Time
(3,4)	DKP1	TUE	1000-1200
(3,4)	DKR2	THU	0800-0900

Lab Hours

Group	Location	Day	Time
(4)	MKY6	MON	1300-1500
(3)	MKY6	MON	1500-1700

Consultation Hours

Group	Location	Day	Time
($)	SME-B10	TUE	1500-1600
($)	SME-B10	WED	1000-1200
($)	SME-B10	WED	1500-1600
($)	SME-B10	THU	1500-1600
($)	SME-B10	FRI	1000-1100

Note The 2-hour slot on Wednesday morning is by appointment only.

Reference

1. Stallings, William. "*Computer Organization and Architecture: Designing for Performance*". 8th Edition, 2010. Prentice Hall.
2. Comer, Douglas E.. "*Essentials of Computer Architecture*". 2005. Prentice Hall.

The first one will most probably be the text-book for this course. The 7th Editions of this book are available at our library. The second one is also interesting to read and I want to use it as reference (good coverage but not enough depth, unfortunately). It is also available at the library.

Course Notes

Chapter 14 - Instruction-Level Parallelism

Superpipelined

- Double-clocked pipeline execution
- almost double the throughput

Superscalar Processors

- processors with multiple execution units (Intel's hyper-threading?) BUT still a single CPU unit
- executing multiple instructions at the same time, subject to true-data dependency issues
- i.e. only works if the'parallel' instructions are processing on different target data