Lab Work 3 - Sequential Logic Circuits

This module consists of a few parts:

1. Latches and Flip-flops
2. One-shots and Oscillators
3. Registers and Counters

Implementing Sequential Logic

Sequential logic circuits mainly provides storage for a digital system. Thus, for example, it allows implementation of processes that need the previous state of a digital logic.

Only two basic types of sequential logic circuit:

- Latch : level-triggered temporary storage device with 2 stable states
- Flip-flop : edge-triggered storage device

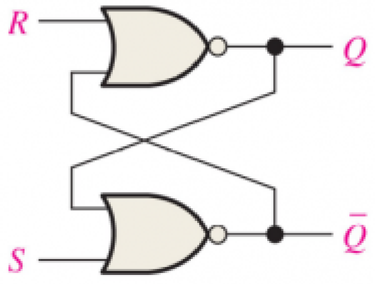
***Note**: We will be using the button (@reset) switch (instead of the normal toggle DIP-switch). Try to find out why this is a better option.*

Implementing Latches

For a basic latch, it needs to have the means to achieve any stable state (HI or LO) at its output and to maintain that output state.

S-R Latch

A basic S-R Latch:



Truth table:

S	R	Q_n	$\overline{Q}_n$
0	0	$Q_{n\text{-}1}$	$\overline{Q}_{n\text{-}1}$
0	1	0	1
1	0	1	0
1	1	0*	0*

Note: '' indicates invalid condition*

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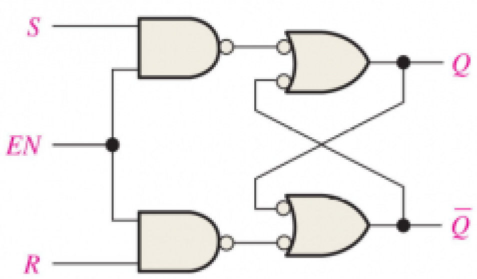
Notice that the invalid condition will happen when the S & R inputs are both at logic 1. In a real digital system, we need to prevent this from happening.

Gated S-R Latch

A gated S-R Latch:



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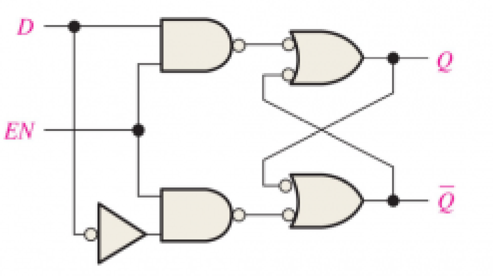
Truth table for a S-R Latch:

S	R	EN	Q_n	$\overline{Q_n}$
0	0	0	Q_{n-1}	$\overline{Q_{n-1}}$
0	1	0	Q_{n-1}	$\overline{Q_{n-1}}$
1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$
1	1	0	Q_{n-1}	$\overline{Q_{n-1}}$
0	0	1	Q_{n-1}	$\overline{Q_{n-1}}$
0	1	1	0	1
1	0	1	1	0
1	1	1	**1**	**1**

*Note:Output in **BOLD** is an invalid condition.*

Gated D Latch

A gated D Latch:



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Truth table for a gated D Latch:

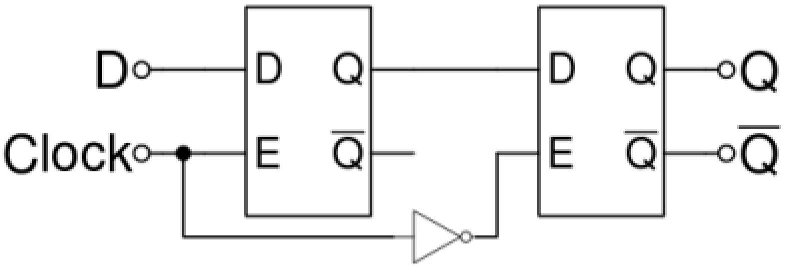
EN	D	Q_n	$\overline{Q_n}$
0	X	Q_{n-1}	$\overline{Q_{n-1}}$
1	0	0	1
1	1	1	0

Implementing Flip-flops

Unlike latches, flip-flops requires *reference* clock signal that is used to transfer whatever signal at its input to its internal storage (latch).

D Flip-flop

A D flip-flop (DFF) can be built using two opposite level-triggered gated D latches. This is known as a master slave DFF, as shown in figure below. Is this a positive or negative edge-triggered DFF?



Disclaimer: *The image above is obtained from Wikipedia*

Truth table for a positive edge-triggered DFF:

CLK	D	Q_n	$\overline{Q_n}$
0→1	0	0	1
0→1	1	1	0

The table for negative edge-triggered DFF onlly differs at CLK column with 1→0 instead of 0→1.

J-K Flip-flop

Truth table for a J-K Flip-flop:

J	K	CLK	Q_n	$\overline{Q_n}$
0	0	0→1	Q_{n-1}	$\overline{Q_{n-1}}$
0	1	0→1	0	1
1	0	0→1	1	0
1	1	0→1	$\overline{Q_{n-1}}$	Q_{n-1}

Notice that, unlike DFF, J-K FF has a toggle mode.

T Flip-flop

The DFF can easily be modified to act as a Flip-flop that toggles on clock edges - by simply connecting the $\overline{Q}$ output to the D input.

Things To Do

THING1 Build an S-R Latch (use NOR gates) and verify.

THING2 Build a gated S-R Latch (use NAND gates) and verify.

THING3 Build a gated D Latch and verify.

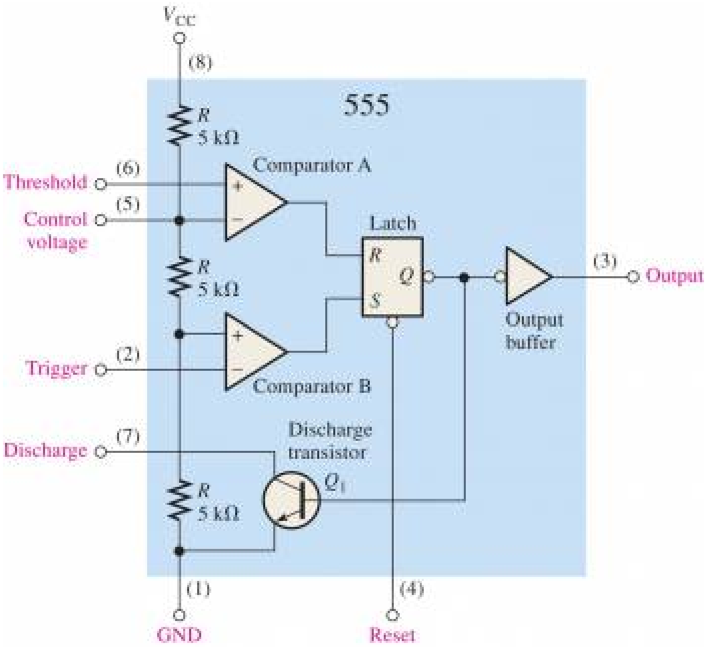
THING4 Build a D Flip-flop (DFF) and verify.

THING5 Build a J-K Flip-flop and verify.

THING6 (optional) Try to verify the use of DFF as a frequency divider.

One-Shots and Oscillators

We will be using the versatile 555 timer as both a monostable multivibrator (one-shot) and an astable multivibrator (oscillator). The internals of a 555 IC is shown below.



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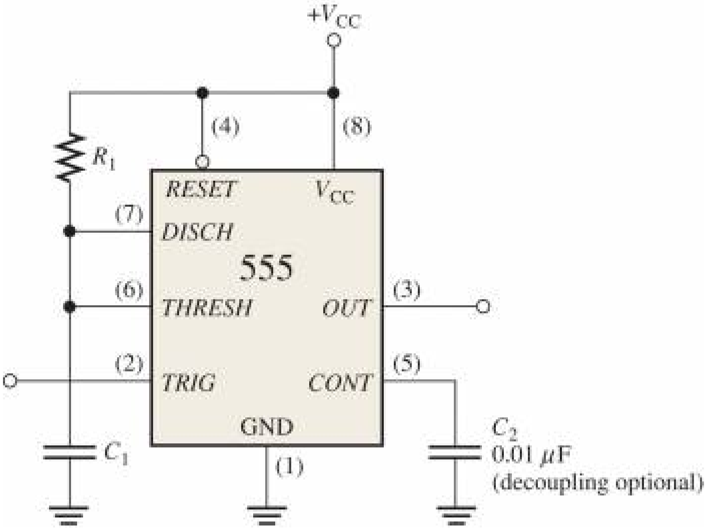
The main internal components of a 555 timer are 2 voltage comparators that are configured by a voltage divider circuit that provides a trigger value of $\frac{1}{3}V_{cc}$ and a threshold value of $\frac{2}{3}V_{cc}$. These values can be externally adjusted using the control voltage pin (5).

555 One-shot Operation

We just need a resistor and a capacitor for this (an extra decoupling capacitor is optional).



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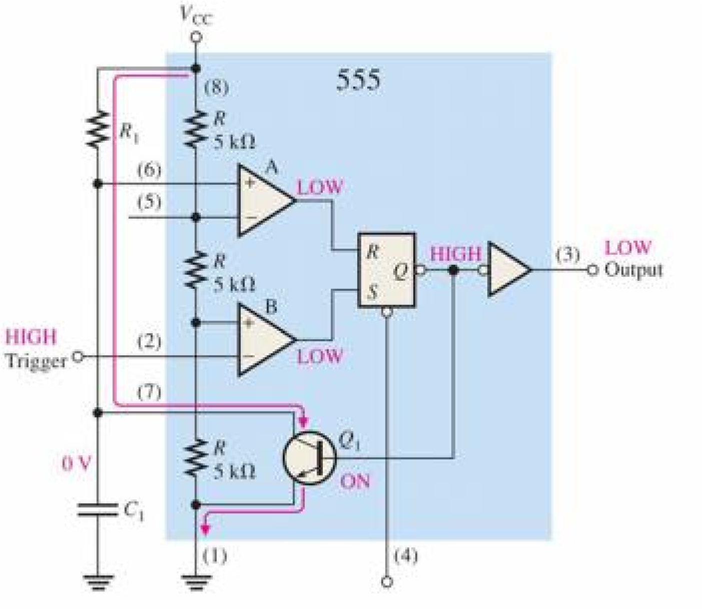
Initially, the circuit will settle down to its stable state.



(a) Prior to triggering. (The current path is indicated by the red arrow.)

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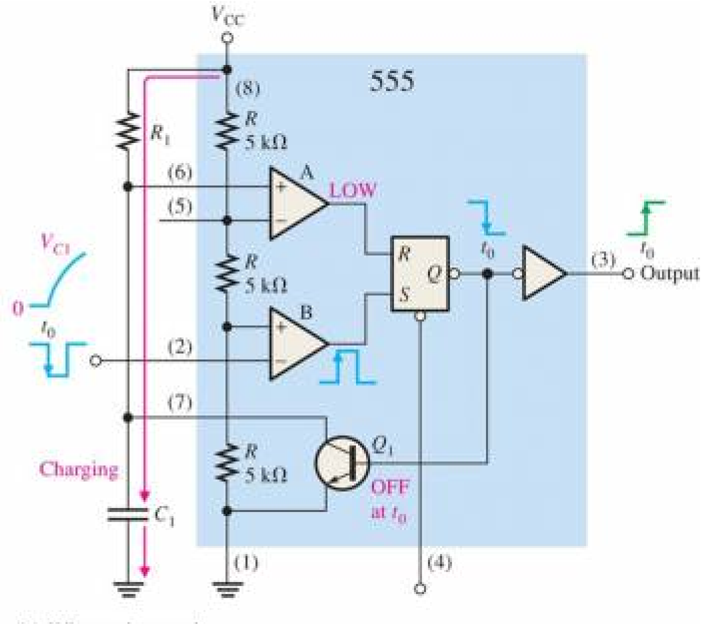
When triggered, it will set the internal R-S latch, which consequently enables the circuit to charge the capacitor.



(b) When triggered

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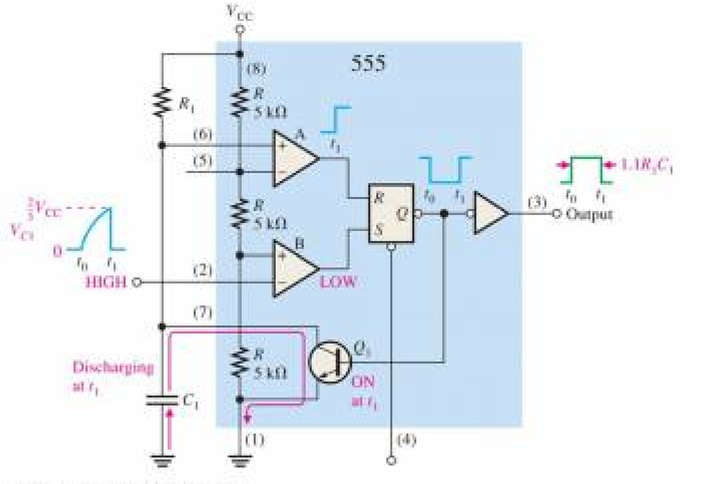
Once the capacitor is fully charged (actually, once the voltage is over threshold) and the trigger signal is deasserted, comparator A should cause the latch to reset and consequently cause the discharging of the capacitor.



(c) At end of charging interval

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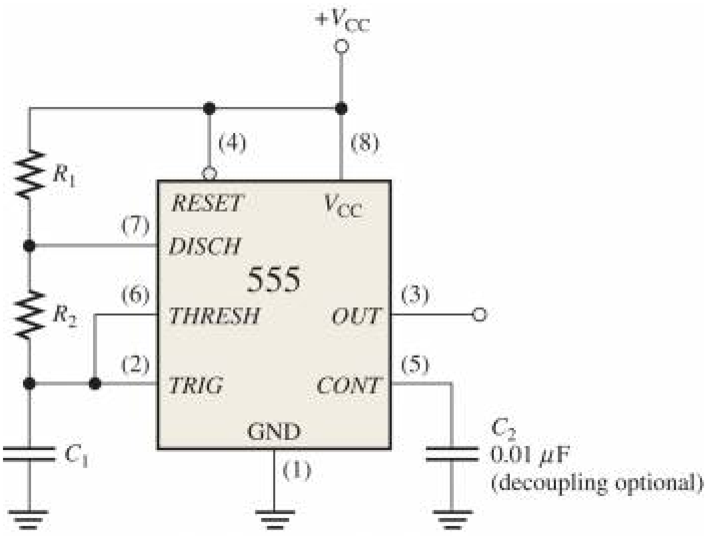
Notice that the pulse width generated at the output pin should be around $t_w = 1.1R_1C_1$

555 Oscillator Operation

This time we need an extra resistor.



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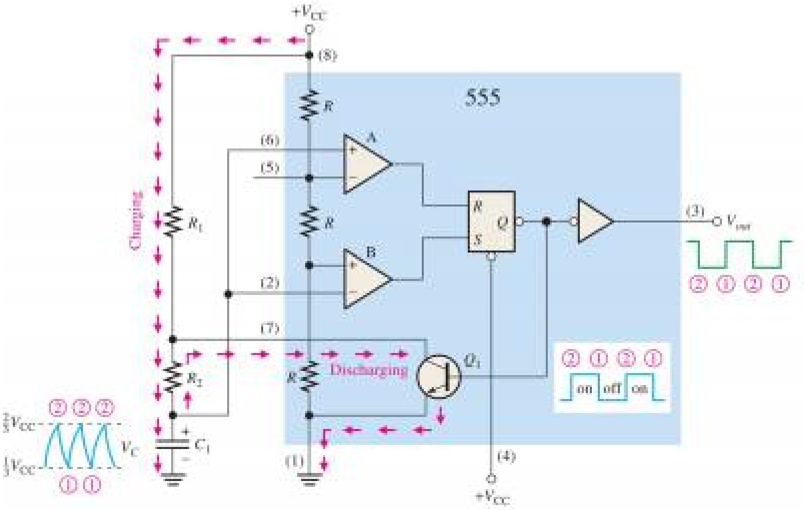
This is how the the oscillator works - the capacitor is charged through the two resistors (R_1 and R_2) when the internal transistor Q_1 is off, and discharged through R_2 when transistor Q_1 is on.



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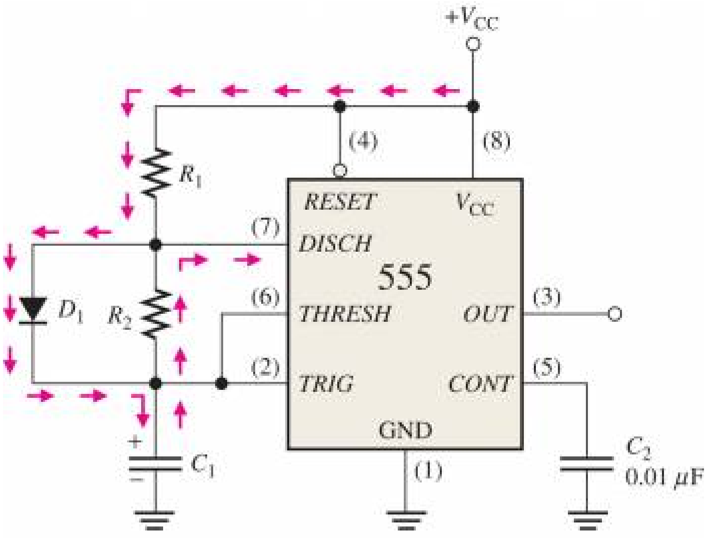
The frequency of the generated signal at the output pin should be $f=\frac{1.44}{\left(R_1+2R_2\right)}C_1$. The time that the output is at V_{CC} should be $t_H=0.7\left(R_1+R_2\right)C_1$, while the time for the output to be at GND should be $t_L=0.7R_2C_1$. Thus, the duty cycle is given by $\left(\frac{R_1+R_2}{R1+2R_2}\right)100\%$.

To get a duty cycle of less than 50%, we need a diode in order to bypass R_2 when charging the capacitor.



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Thus, the duty cycle is now given by $\left(\frac{R_1}{R_1+R_2}\right)100\%$.

Things To Do

THING1 Build a one-shot circuit that produces 1ms pulse. Determine a suitable R & C values. Verify.

THING2 Build an oscillator circuit that produces 1kHz (50% duty cycle) square-wave signal. Verify.

THING3 (Optional) Build an oscillator circuit that produces 50Hz signal, and $t_H = 1ms$. Verify.

Flip-flop ICs

We are going to look at samples of flip-flop IC:

- D Flip-flop (DFF 7474: Dual D-FF positive-edge triggered, asynchronous preset & clear)
- J-K Flip-flop (JKFF 7476: Dual JK-FF asynchronous preset & clear)
- J-K Flip-flop (JKFF 74112: Dual JK-FF negative-edge triggered, asynchronous preset & clear)

Things To Do

THING1 Implement a 2-bit counter (asynchronous, continuously counts up).

THING2 (Optional) Implement **THING1** with start/stop/reset button(s).

THING3 Implement a 4-bit counter (asynchronous, continuously counts up).

THING4 (Optional) Implement a 4-bit counter (asynchronous, continuously counts down).

THING5 Implement a 4-bit running light (**Hint**: Ring Counter - you need a reset switch for this).