MY1CV: Publications

Journal of Physics: Conference Series 2019

Citation: Azman M. Yusof, Ali Yeon Md Shakaff, Saufiah A. Rahim, “Software solution for Testing Image Processing Algorithm on Conveyor-Based Vision Systems”, *Journal of Physics: Conference Series*, Volume 1372, https://iopscience.iop.org/article/10.1088/1742-6596/1372/1/012059

Abstract: Vision systems have been used in many applications that intends to reduce the need for human operators. This is especially true for tasks that are simple but repetitive in nature, which is largely applicable to most manufacturing and agriculture’s post-harvest processes. Many such processes utilize conveyor-based systems where the objects being processed are placed on a conveyor belt that runs through multiple processing stations. Implementing a vision system to capture images of an object that is moving usually requires setting up an imaging device to a working conveyor system. Getting a working conveyor system to be ready can take some time and consequently delay development work on the vision system itself, especially those involving image processing algorithms. This paper proposes a software solution that can be used to expedite initial work on such systems. The solution is written in C and is therefore easily ported to any development machine. A basic image processing library has also been developed so that it does not depend on any development library or suite, which is usually huge in size. Thus, the solution can easily be compiled and run on embedded development boards like Raspberry Pi - for a more portable solution.

JTEC 2018

Citation: Azman M. Yusof, Ali Yeon Md Shakaff, Saufiah A. Rahim, “Implementation of a Hardware-centric Vision System Architecture”, *Journal of Telecommunication, Electronic and Computer Engineering (JTEC)*, Volume 10, No 1-15, Pages 123-129, ISSN 2180-1843, eISSN 2289-8131, https://journal.utem.edu.my/index.php/jtec/article/view/4058

Abstract: Currently, most implementations of vision systems still heavily rely on software - computer algorithms run on general purpose microprocessors, like on personal computers. This is understandable since personal computers (PC) are readily available, and software implementations provide flexibility, especially when trying out various algorithms. The need to have real-time vision-based systems influenced developers and researchers towards hardware-based - or at least hardware-assisted - vision systems that are capable of processing huge amount of data from an imaging device in realtime (i.e. embedded vision system). Platforms like DSPs, GPUs and FPGAs are among the commonly used development platforms for a hardware-centric vision system, while ASIC implementations - tagged with a huge development cost - usually have the best performance. This paper compares various possible platforms that are readily available and can be used to develop hardware-centric vision systems. This includes DSPs, GPUs and FPGAs, with some insights on ASIC implementation. Consequently, two implementations of the proposed hardwarecentric vision system architecture are presented. Both implementations managed to process incoming image stream from camera module at 30 frames per second.

Neurocomputing 2014

Citation: Saufiah A. Rahim, Azman M. Yusof, Thomas Bräunl, “Genetically evolved action selection mechanism in a behavior-based system for target tracking”, *Neurocomputing*, Volume 133, 10 June 2014, Pages 84-94, ISSN 0925-2312, https://dx.doi.org/10.1016/j.neucom.2013.11.028.

Abstract: The success of a behavior-based system relies largely on its Action Selection Mechanism (ASM) module, which is basically a behavior coordination method of either arbitration or command fusion type. Deciding on the right coordination method for ASM when executing a given mission in an arbitrary environment can be a huge obstacle. Providing the system with some kind of Artificial Intelligence (AI) to deal with the dynamics of a given task would be highly recommended. In this paper, an evolutionary process has been employed in a behavior-based system to generate a suitable ASM based on a system's mission scenario. A Genetic Algorithm (GA) is used to train the weights of a Multi-layer Perceptron (MLP) feed-forward artificial neural network in identifying a suitable formulation of ASM. Implementation of such systems in a target tracking mission has shown positive results. Depending on the mission scenario, the evolved ASM can dynamically manage the coordination method in order to achieve the overall system objective.

ROVISP (2007) - International Conference on Robotics, Vision, Information and Signal Processing

ISBN: 978-983-43178-1-2

Citation: Azman M.Yusof and Thomas Braunl, “Using Xilinx ML310 Development Board as Test and Development Platform for FPGA-based Embedded Vision System”, pp. 350-353.

Abstract: FPGA-based embedded vision systems are currently the natural option for many vision system researchers and developers. The design and fabrication of a customized FPGA-based board for embedded vision system could be time-consuming and require proper verification of the functionality of the board itself, before using it for its actual task. As an alternative, a ready-for-testing system is usually available in the form of development board like the Xilinx ML310 Development Board. Other than the basic serial communication ports for desktop PC interface, it also has a 256MB DDR SDRAM available. This is very useful when building systems for image processing tasks. A simple custom interface board to a CMOS camera and an LCD display has been fabricated for this purpose. The advantages and the disadvantages of using this development board as a test and development platform will be discussed.

International Journal of Electronics (2001)

ISSN:0020-7217

Citation: S. M. Rezaul Hasan, Lim Chu Aun and Azman Yusof, “600 MHz BiCMOS digitally controlled oscillator for clock recovery & frequency synthesis PLLs”, *International Journal of Electronics*, Taylor & Francis, U.K., vol. 88, no. 5, pp. 529-541, May 2001.

Abstract: A 16-bit digitally controlled BiCMOS ring oscillator (DCO) is described. This BiCMOS DCO

design provides improved frequency stability under thermal fluctuations. Simulations of a 5-stage DCO using 1 µm BiCMOS process parameters achieved a controllable frequency range of 90-640 MHz with a linear/quasi-linear range of around 300 MHz. A tiny test chip was fabricated using MOSIS Orbit 2 µm low-cost analogue CMOS process technology that provides a lateral NPN bipolar device option Monotone frequency gain (frequency vs control-word transfer function) with fine stepping (tuning) over several kHz was verified experimentally, thus auguring the prospect of accurate frequency lock in an all-digital phase-locked loop (ADPLL) application Worst-case jitter due to digital control transitions at pathological control-word boundaries for the BiCMOS DCO was observed to be less than 50 ps. This BiCMOS design would thus provide performance enhancement in PLL applications such as clock recovery and frequency synthesis.

IEEE National Symposium on Microelectronics (NSM2001)

Citation: Azman M. Yusof, Ali Yeon Md. Shakaff, Mohd. Noor Ahmad, “Implementation of a Cascadable Neural Processor for Pattern Classification Engine in an Artificial Taste Sensing System”, *2001 IEEE National Symposium on Microelectronics*, 12-13 Nov 2001, Awana Genting Highlands, Malaysia.

Abstract: An implementation of a 16-bit floating-point neuron-like neural processor, known as NEWRON, is presented. NEWRON implements the Multi-Layer Perceptron (MLP) neural network algorithm, with on-chip back-error propagation (BEP) training. It is primarily intended to be the prototype model for a real-time pattern classification engine in an artificial taste/smell sensing application, which is currently being developed. The use of 16-bit floating-point data format increases the dynamic range of calculated digital values. The standard MLP with BEP algorithm has been restructured into an object-oriented algorithm (OOA). In simple words, each NEWRON has a slightly modified algorithm that enables it to independently store and manage all parameters (weight, bias and node values) related to it. OOA also enables NEWRON to accommodate the insertion of the sliding feeder technique, which reduces the complexity of common neural network interconnections. Serial transmissions are used to exchange data between cascaded NEWRONs. The speed of the serial transmission does not affect the network because it is done while the time consuming floating-point calculation takes place.

Citation: Azman M. Yusof, “16-bit Floating-point Arithmetic Unit for Customized Data Processing Unit”, *2001 IEEE National Symposium on Microelectronics*, 12-13 Nov 2001, Awana Genting Highlands, Malaysia.

Abstract: The design of a floating-point arithmetic unit, to be used in a fully customized data processing unit, is presented. It has been designed for a full-custom neural network engine. A 16-bit floating-point data format, which is based on the IEEE 32-bit floating-point data format, has been adopted. Though it has limited accuracy compared to the latter, it offers a wider dynamic range compared to a fixed-point data of equivalent length. When implemented using minimum-sized devices in full-custom static logic cells, at 3.3V power supply, in a 1.2µ CMOS process, the 16-bit floating-point arithmetic unit is capable of around 8.3 MFLOPS (millions floating-point operations per second).

Great Lakes Symposium on VLSI (GLS98)

ISBN:0-8186-8409-7, pp. 71-71

Citation: Azman M. Yusof, S.M. Rezaul Hasan, Lim Chu Aun, “600 MHz Digitally Controlled BiCMOS Oscillator (DCO) for VLSI Signal Processing & Communication Applications”, *Great Lakes Symposium on VLSI ’98*, 19-24 Feb 1998, Lafayette, Louisiana.

Abstract: A 16-bit digitally controlled BiCMOS ring oscillator (DCO) is described. This BiCMOS DCO design provides improved frequency stability under thermal fluctuations compared to a CMOS DCO design. Simulations of a 5-stage DCO using a 1-um BiCMOS process parameters achieved a controllable frequency range of 90-640 MHz with a linear/quasi-linear range of around 300MHz. Monotone frequency gain (frequency vs control word transfer function) with fine stepping (tuning) in several KHz was verified. This augurs the prospect of accurate frequency lock in a BiCMOS all digital PLL (ADPLL) application in digital VLSI communication systems. Worstcase jitter due to digital control transitions at pathological control word boundaries for the BiCMOS DCO was observed to be less than 50 ps, which is lower than that for the CMOS DCO.