Display Modules

Dumped...

P10 Matrix Display

Useful info for development

info_p10_display.txt

```
Interface pins:
[A]
[B]
[CLK]
[SCLK]
[R]
[OE]

16-bit Ribbon-Cable Port:
[nOE:  A]
[GND:  B]
[GND:N/A]
[GND:SCK]
[GND:LCK]
[GND:  R]
[GND:N/A]
[GND:N/A]

Devices:

- 74HC245: octal 3-state non-inverting bus tranceivers
  = 20-pins
  > vcc & gnd (pins 20 & 10)
  > A1-A8 (pins 2-10)
  > B1-B8 (pins 11-18)
  > DIR (pin 1)
  > OE' (pin 19)
  = when OE=1: all signal pins (A1-A8,B1-B8) tri-stated
  = when DIR=1: A->B, DIR=0: A<-B
  = interface layer
  > [A] <> A1
  > [B] <> A2
  > [OE] <> A3
  > [CLK] <> A4,A5
  > [SCLK] <> A6,A7
  > [R] <> A8
```

```
- 74HC138: 3-8 decoder with active low outputs
  = 16-pins
  > vcc & gnd (pins 16 & 8)
  > A0-A2 (pins 1-3)
  > Y0-Y7 (pins 15-9,7)
  > G0',G1',G2 (pins 4-6) : enable pins
  = interface layer
  > [A] <> A0
  > [B] <> A1
  > [OE]' <> G1' ([OE]' is output of 7404 hex inv)
  > GND <> A2
  > GND <> G0'
  > VCC <> G2
  = basically, only Y0-Y3 will be active based on {B,A} value

- 74HC595: 8-bit shift registers with 3-state output resgisters
  = data loader @shifter
  = 16-pins
  > vcc & gnd (pins 16 & 8)
  > QA-QH,QH' (pins 15,1-7,9)
  > SER (pin 14) : serial in
  > OE' (pin 13)
  > RCLK (pin 12) : output register clock (+ve edge)
  > SRCLK (pin 11) : shift register clock (+ve edge)
  > SRCLR' (pin 10) : shift register CLR ((active low)
  = note: RCLK & SRCLK should be non-overlapping
  = interface layer
  > [CLK] <> SRCLK
  > [SCLK] <> RCLK
  > GND <> OE'
  > VCC <> SRCLR'
  > [R] <> SER
  > [next-SER] <> QH'
```

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