Introduction to Verilog and ModelSim

This page is intended for the participants of 'Introduction to Verilog and ModelSim' training course (July 19-21, 2016).

Updated20160718: The course has been postponed to August 1-3, 2016.

Many electronic system design work involves Hardware Description Language (HDL) coding. Verilog HDL is one of the easiest HDL to learn and is the preferred language especially for entry-level engineers. This is because of its simplicity (e.g. as opposed to VHDL which is strongly typed) and its C-like syntax (which most engineering students would be familiar with). ModelSim is an industry-standard HDL simulation environment by Mentor Graphics® that is used (among others) for Integrated Circuit (IC) design, FPGA-based digital designs, or simply for logic verification.

Course Objectives

This course is designed to provide introductory-level practical knowledge on using Verilog and ModelSim for simple digital logic/system design.

Learning Outcomes

Upon completion of this course, the participants should be able to:

1. Understand the basic requirements in implementing digital design using HDL
2. Create and implement a simple digital logic design using Verilog
3. Test and verify a simple digital logic design using ModelSim

Who Will Benefit From This Course

This course is designed for engineers, researchers, system designers, technical specialists, graduate students and individuals who are interested in developing fundamental skills on digital systems development, especially on FPGA platform.

Related keywords: HDL, Verilog, ModelSim, Digital Logic/Systems Design.

Course Content

Sessions	Details	Materials	Notes

Session 1	• Introduction to Verilog
	  ◦ Overall view on CAD-based design flow
	  ◦ Introduction to HDLs
	  ◦ Introduction to Digital Simulation Tool
	  ◦ Implementing simple logic design using Verilog
	  ◦ Implementing simple testbench using Verilog
		Slide 1
		Slide 2
			Mainly a theoretical session

Session 2	• Using ModelSim
	  ◦ Creating a new project on ModelSim
	  ◦ Add/create Verilog files to the project
	  ◦ Run simulation using ModelSim
	  ◦ Analyze waveform based on simulation results
		Slide 3	Step-by-step software session

Session 3 & 4	• Combinational Logic ◦ Moving towards designing an ALU	Slide 4	A more practical session (2 slots)

Session 5 & 6	• Sequential Logic
	  ◦ Moving towards designing a register block
	(This is optional and depends on participants' progress)
	• State Machines and Control Logic
	  ◦ Moving towards designing control block
		Slide 5
		Slide 6
		(Optional)
			A more practical session (2 slots)