8080A/8085A INSTRUCTION SET INDEX

Instruction	Code	Bytes	T States		Machine Cycles
			8085A	8080A	
ACI DATA	CE data	2	7	7	F R
ADC REG	1000 1SSS	1	4	4	F
ADC M	8E	1	7	7	F R
ADD REG	1000 0SSS	1	4	4	F
ADD M	86	1	7	7	F R
ADI DATA	C6 data	2	7	7	F R
ANA REG	1010 0SSS	1	4	4	F
ANA M	A6	1	7	7	F R
ANI DATA	E6 data	2	7	7	F R
CALL LABEL	CD addr	3	18	17	S R R W W*
CC LABEL	DC addr	3	9/18	11/17	S R▪/S R R W W*
CM LABEL	FC addr	3	9/18	11/17	S R▪/S R R W W*
CMA	2F	1	4	4	F
CMC	3F	1	4	4	F
CMP REG	1011 1SSS	1	4	4	F
CMP M	BE	1	7	7	F R
CNC LABEL	D4 addr	3	9/18	11/17	S R▪/S R R W W*
CNZ LABEL	C4 addr	3	9/18	11/17	S R▪/S R R W W*
CP LABEL	F4 addr	3	9/18	11/17	S R▪/S R R W W*
CPE LABEL	EC addr	3	9/18	11/17	S R▪/S R R W W*
CPI DATA	FE data	2	7	7	F R
CPO LABEL	E4 addr	3	9/18	11/17	S R▪/S R R W W*
CZ LABEL	CC addr	3	9/18	11/17	S R▪/S R R W W*
DAA	27	1	4	4	F
DAD RP	00RP 1001	1	10	10	F B B
DCR REG	00SS S101	1	4	5	F*
DCR M	35	1	10	10	F R W
DCX RP	00RP 1011	1	6	5	S*
DI	F3	1	4	4	F
EI	FB	1	4	4	F
HLT	76	1	5	7	F B
IN PORT	DB data	2	10	10	F R I
INR REG	00SS S100	1	4	5	F*
INR M	34	1	10	10	F R W
INX RP	00RP 0011	1	6	5	S*
JC LABEL	DA addr	3	7/10	10	F R/F R R†
JM LABEL	FA addr	3	7/10	10	F R/F R R†
JMP LABEL	C3 addr	3	10	10	F R R
JNC LABEL	D2 addr	3	7/10	10	F R/F R R†
JNZ LABEL	C2 addr	3	7/10	10	F R/F R R†
JP LABEL	F2 addr	3	7/10	10	F R/F R R†
JPE LABEL	EA addr	3	7/10	10	F R/F R R†
JPO LABEL	E2 addr	3	7/10	10	F R/F R R†
JZ LABEL	CA addr	3	7/10	10	F R/F R R†
LDA ADDR	3A addr	3	13	13	F R R R
LDAX RP	000X 1010	1	7	7	F R
LHLD ADDR	2A addr	3	16	16	F R R R R

Instruction	Code	Bytes	T States		Machine Cycles
			8085A	8080A	
LXI RP,DATA 16	00RP 0001 data16	3	10	10	F R R
MOV REG,REG	01DD DSSS	1	4	5	F*
MOV M,REG	0111 0SSS	1	7	7	F W
MOV REG, M	01DD D110	1	7	7	F R
MVI REG, DATA	00DD D110 data	2	7	7	F R
MVI M, DATA	36 data	2	10	10	F R W
NOP	00	1	4	4	F
ORA REG	1011 0SSS	1	4	4	F
ORA M	B6	1	7	7	F R
ORI DATA	F6 data	2	7	7	F R
OUT PORT	D3 data	2	10	10	F R O
PCHL	E9	1	6	5	S*
POP RP	11 RP 0001	1	10	10	F R R
PUSH RP	11 RP 0101	1	12	11	S W W*
RAL	17	1	4	4	F
RAR	1F	1	4	4	F
RC	D8	1	6/12	5/11	S/S R R*
RET	C9	1	10	10	F R R
RIM (8085A only)	20	1	4	-	F
RLC	07	1	4	4	F
RM	F8	1	6/12	5/11	S/S R R*
RNC	D0	1	6/12	5/11	S/S R R*
RNZ	C0	1	6/12	5/11	S/S R R*
RP	F0	1	6/12	5/11	S/S R R*
RPE	E8	1	6/12	5/11	S/S R R*
RPD	E0	1	6/12	5/11	S/S R R*
RRC	0F	1	4	4	F
RST N	11XX X111	1	12	11	S W W*
RZ	C8	1	6/12	5/11	S/S R R*
SBB REG	1001 1SSS	1	4	4	F
SBB M	9E	1	7	7	F R
SBI DATA	DE data	2	7	7	F R
SHLD ADDR	22 addr	3	16	16	F R R W W
SIM (8085A only)	30	1	4	-	F
SPHL	F9	1	6	5	S*
STA ADDR	32 addr	3	13	13	F R R W
STAX RP	000X 0010	1	7	7	F W
STC	37	1	4	4	F
SUB REG	1001 0SSS	1	4	4	F
SUB M	96	1	7	7	F R
SUI DATA	D6 data	2	7	7	F R
XCHG	EB	1	4	4	F
XRA REG	1010 1SSS	1	4	4	F
XRA M	AE	1	7	7	F R
XRI DATA	EE data	2	7	7	F R
XTHL	E3	1	16	18	F R R W W

Machine cycle types:

F	Four clock period instr fetch
S	Six clock period instr fetch
R	Memory read
I	I/O read
W	Memory write
O	I/O write
B	Bus idle
X	Variable or optional binary digit
DDD	Binary digits identifying a destination register B=000, C=001, D=010, Memory=110
SSS	Binary digits identifying a source register E=011, H=100, L=101, A=111
RP	Register Pair BC=00, HL=10, DE=01, SP=11

* Five clock period instruction fetch with 8080A

† The longer machine cycle sequence applies regardless of condition evaluation with 8080A

▪ An extra READ cycle (R) will occur for this condition with 8080A