NMK20603

Computer Architecture

MY1

Verilog Basics

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😎 Note:

- mainly, Verilog95!
- some 2K1 (will state)

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Describe:

A logic block

3 Input 1 Output

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Schematic!

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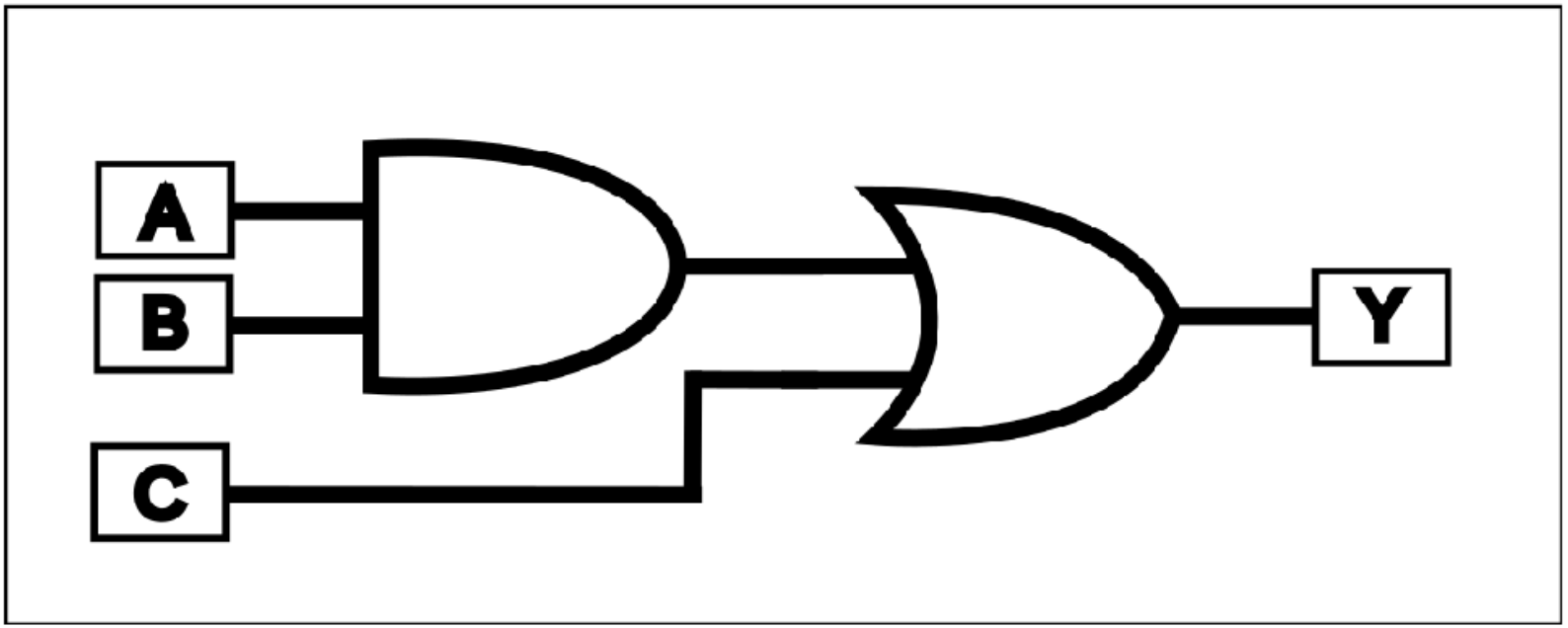
mylogic



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Basic Construct: Module!

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```
module mylogic ();
endmodule
```

Parenthesis holds port list (csv)

Describe:

Ports!

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```
module mylogic (a,b,c,y);
endmodule
```

Ports can be:

- input
- output
- inout

Use input &

output ONLY!

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Describe:

Port Types!

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```
module mylogic (a,b,c,y);
input a,b,c;
output y;
endmodule
```

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Describe:

Logic Elements!

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Data types

- net (keyword:wire)
- variable (keyword: reg)

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Keywords

- assign (wire)
- always/initial (reg)

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RULE:

comb. logic

use assign/wire only!

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always/reg

only for seq. logic

(and tb)

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RULE:

allowed operators

AND, OR, INV

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```
module mylogic (a,b,c,y);
input a,b,c;
output y;
wire y;
assign y = (a & b) | c;
endmodule
```

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RULE:

2-input logic gates ONLY

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Need temporary signal ⇒ wire!

```
module mylogic (a,b,c,y);
input a,b,c;
output y;
wire y, t;
assign t = a & b;
assign y = t | c;
endmodule
```

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RULE:

All signals @wire must be declared!

Done...

⇒ save file!

RULE:

1 file 1 module

RULE:

file name ===

module name (.v)

How to test?

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Imagine:

Breadboard Testing

logic gate (IC)

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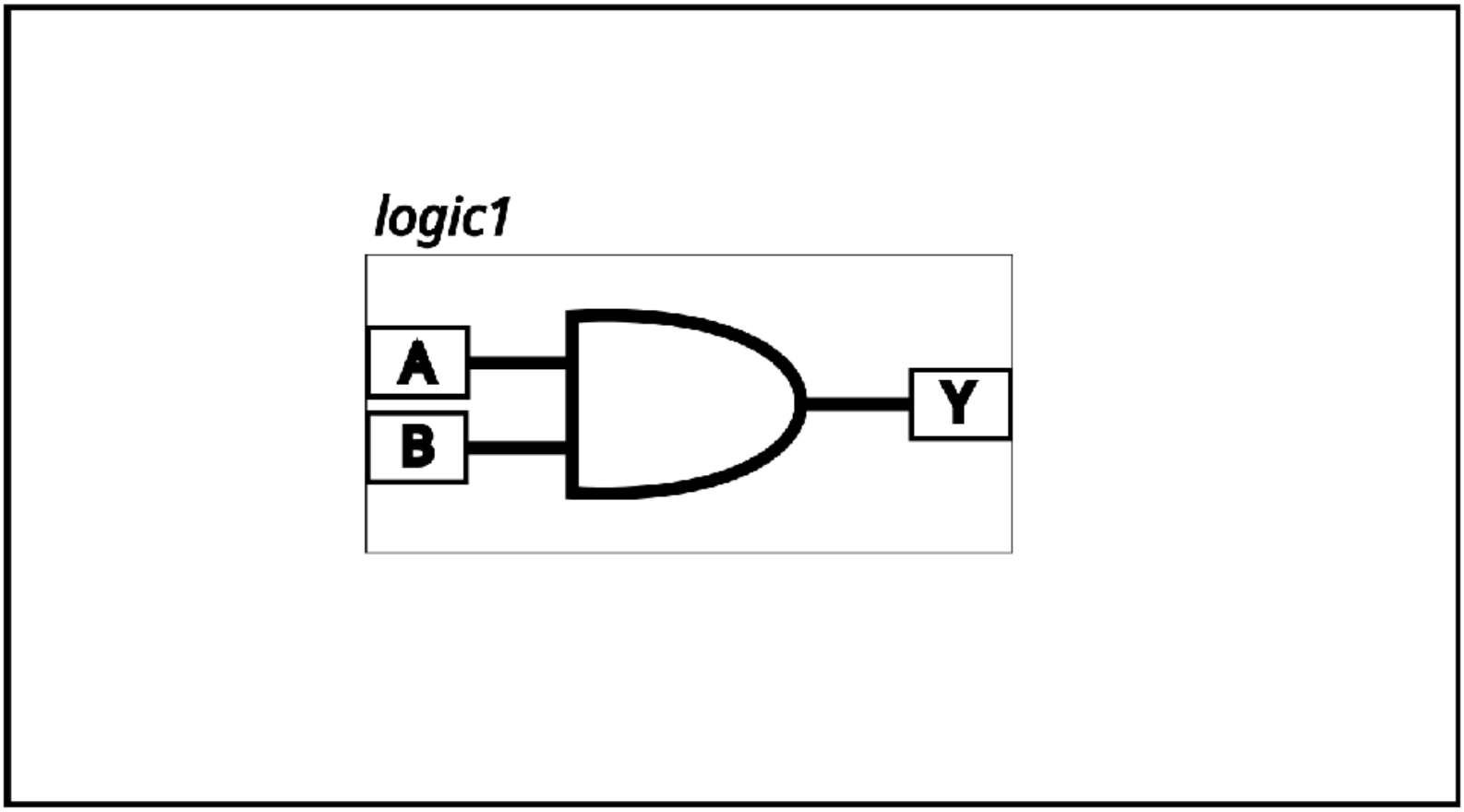
test?



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...

⇒ generate stimuli

⇒ monitor reponse

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RULE:

All module MUST have a testbench

A testbench (tb)

is also a module!

RULE:

Tb name ===

module name + _tb

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Schematic!

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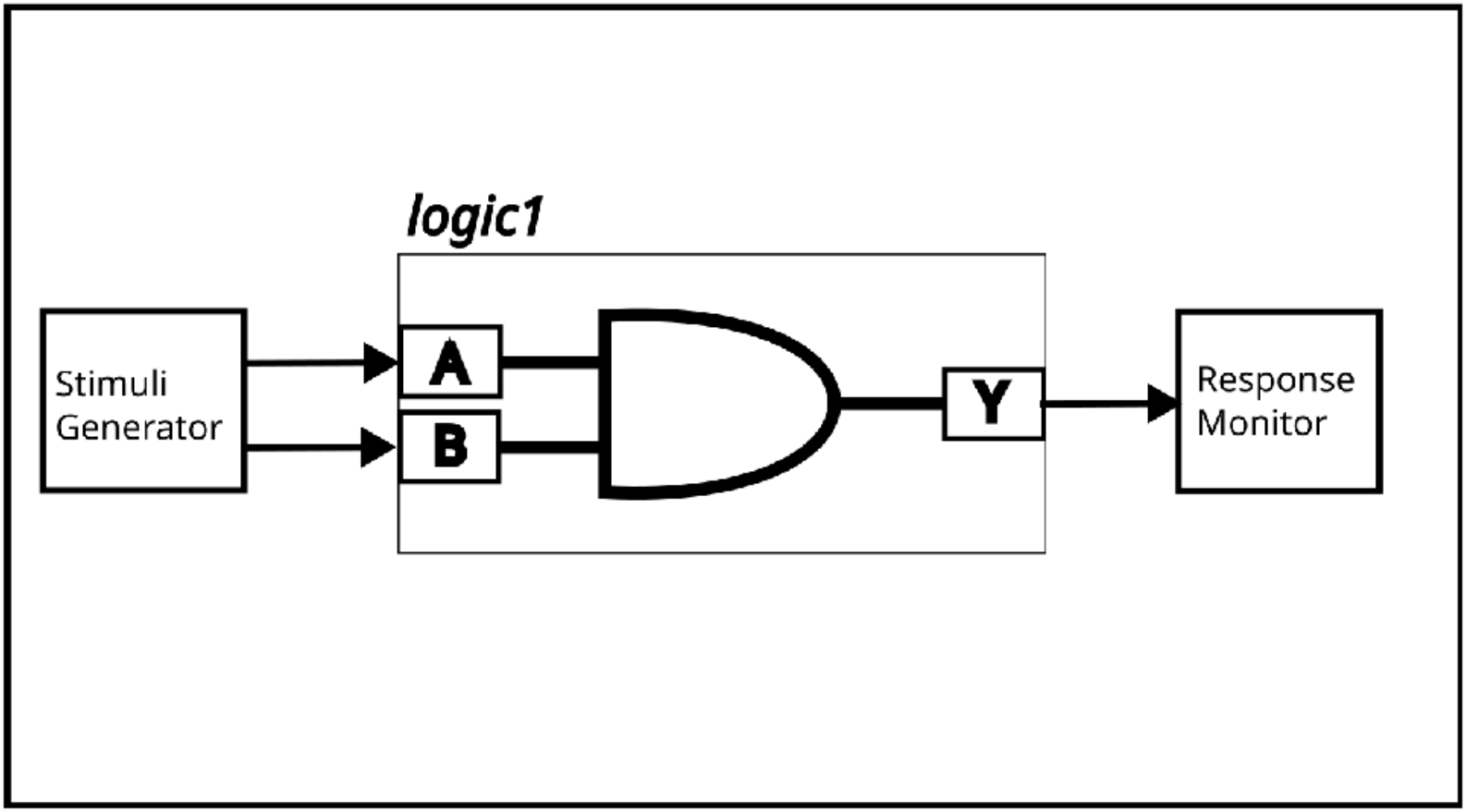
logic1_tb



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Describe:

Testbench

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```
module mylogic_tb ();
endmodule
```

Tb needs

NO PORT!

Design Hierarchy:

Instantiate a module

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```
module mylogic_tb ();
mylogic dut (P,Q,R,Z);
endmodule
```

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RULE:

Port connection(s)

by ordered list ONLY!

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- dut === design under test

Specify

Tb nets

@ 'variables'

```
module mylogic_tb ();
reg P,Q,R; // dut inputs
wire Z; // dut output
mylogic dut (P,Q,R,Z);
endmodule
```

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Describe:

Stimuli 'Generator'

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Keyword

- initial
  - ⇒ like always, but once
  - → block: begin & end

```
module mylogic_tb ();
reg P,Q,R;
wire Z;
initial
begin
end
mylogic dut (P,Q,R,Z);
endmodule
```

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Input Sequence Generator?

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Needs:

- loop counter

Keyword

- integer (not int!)

```
module mylogic_tb ();
reg P,Q,R;
wire Z;
integer loop;
initial
begin
  for (loop=0;loop<8;loop=loop+1)
  begin
  end
end
end
mylogic dut (P,Q,R,Z);
endmodule
```

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Connect input

3x1-bit as 3-bit?

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Syntax

- {} pair

⇒ concatenation op

```
module mylogic_tb ();
reg P,Q,R;
wire Z;
integer loop;
initial
begin
  for (loop=0;loop<8;loop=loop+1)
  begin
    {P,Q,R} = loop;
    #10; // delay to 'see' change! TU!
  end
end
mylogic dut (P,Q,R,Z);
endmodule
```

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delay (#) is in

variable TU (time-unit)

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Done...

⇒ save file!

Homework:
Verilog code for given logic

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0