

NMK20603

Computer Architecture

Codes so far:

✓ alu_4b

✓ regblock4

✓ ringctr4

Describing Simple Digital System

State Machine
incomplete...

State/Sequence:

⇒ S1: get code

⇒ S2: read reg

⇒ S3: process

⇒ S4: write reg

Completing Output (@Control) Logic

- ✓ rs1_enb,rs2_enb, rd0_enb
 - ✓ rs1_add,rs2_add, rd0_add
 - ✓ alu_sel
- ⇒ 'hidden' lines

Processor Core (Top level)

- ✓ 4b processor

- ⇒ @4b data bus

- ✓ 4 x 4b registers

Input Logic?

Instruction!

✓ sizeof inst

⇒ sizeof bus

Let's do 8!

Instruction Set Architecture (ISA)

✓ register move

⇒ 1+2 params @ info

✓ alu operation

⇒ 1+3 params

✓ register load...

⇒ 1+2 params

ISA design

- ✓ bits for inst id
- ✓ bits for param1
- ✓ bits for param2
- ✓ bits for param3

Completing State Machine (and core!)

Note:

✓ state transition @-ve clk

⇒ dffepc write @+ve clk

✓ dreg @regblock write @+ve clk

⇒ dual clock? inv!

Describe:

upcore

✓ iclk,irst,ienb,inst

✓ ostt,done

Testbench?

Describe:
upcore_tb