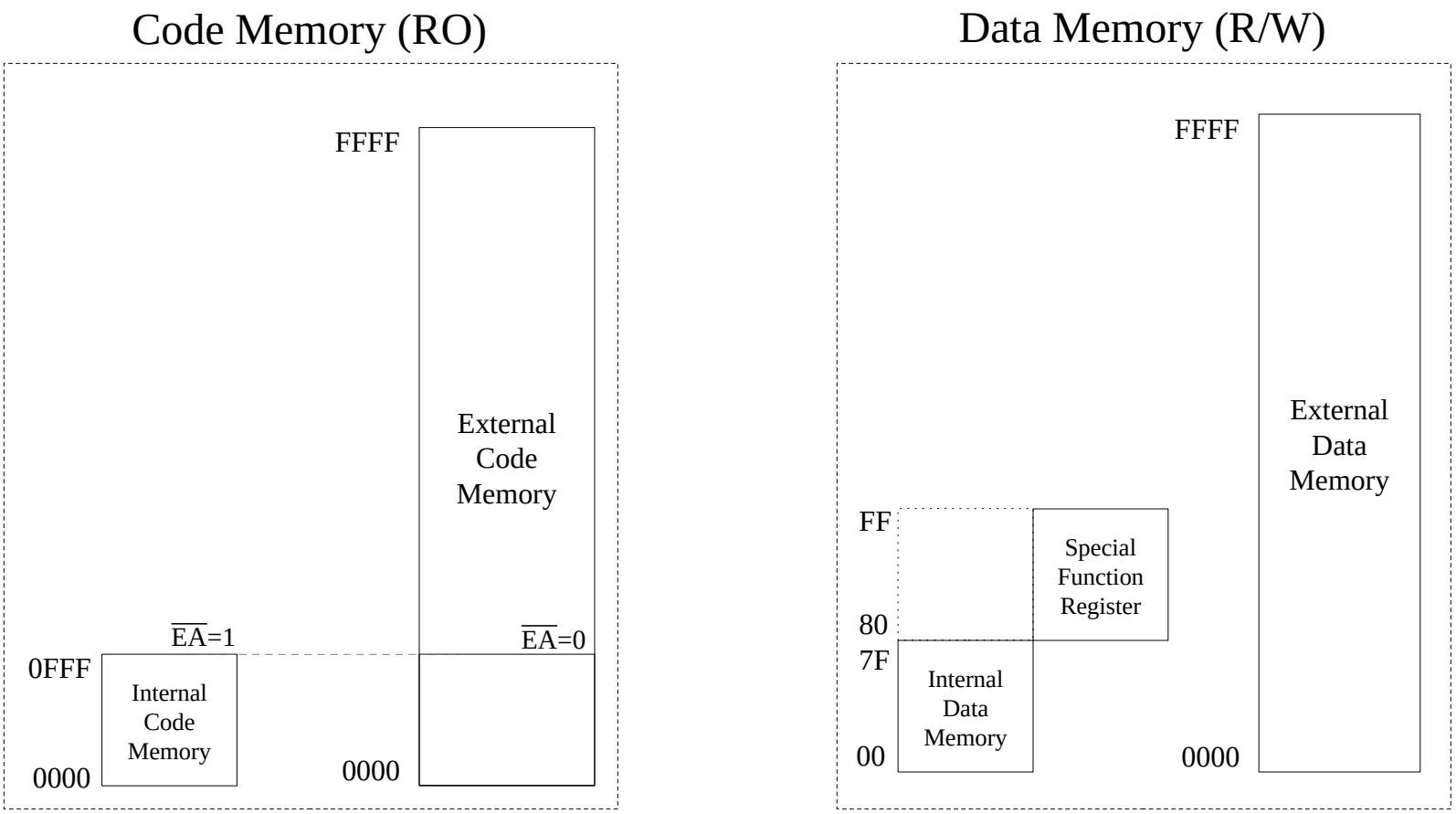
NMK322 - Microcontroller

Lecture 02 – Architecture

8051 Architecture

8051: Memory Organization



Code Memory

- on startup/reset, 8051 fetch instruction @0000H
  - depends on $\overline{EA}$ pin: 0000H can point to internal code memory ($\overline{EA}$=1) or external ($\overline{EA}$=0)

Data Memory

- Internal (128 bytes)
  - 4 banks of 8x8-bit registers (first 32 bytes)
  - active bank accessed as R0-R7
  - bit addressable registers @20H-2FH
  - the others can be accessed as RAM
  - note:stack also utilize these space

30 – 7F	General Purpose Ram							
2F	7F	7E	7D	7C	7B	7A	79	78
2E	77	76	75	74	73	72	71	70
2D	6F	6E	6D	6C	6B	6A	69	68
2C	67	66	65	64	63	62	61	60
2B	5F	5E	5D	5C	5B	5A	59	58
2A	57	56	55	54	53	52	51	50
29	4F	4E	4D	4C	4B	4A	49	48
28	47	46	45	44	43	42	41	40
27	3F	3E	3D	3C	3B	3A	39	38
26	37	36	35	34	33	32	31	30
25	2F	2E	2D	2C	2B	2A	29	28
24	27	26	25	24	23	22	21	20
23	1F	1E	1D	1C	1B	1A	19	18
22	17	16	15	14	13	12	11	10
21	0F	0E	0D	0C	0B	0A	09	08
20	07	06	05	04	03	02	01	00
18 – 1F	Register Bank 3							
10 – 17	Register Bank 2							
08 – 0F	Register Bank 1							
00 – 07	Register Bank 0							

SFR

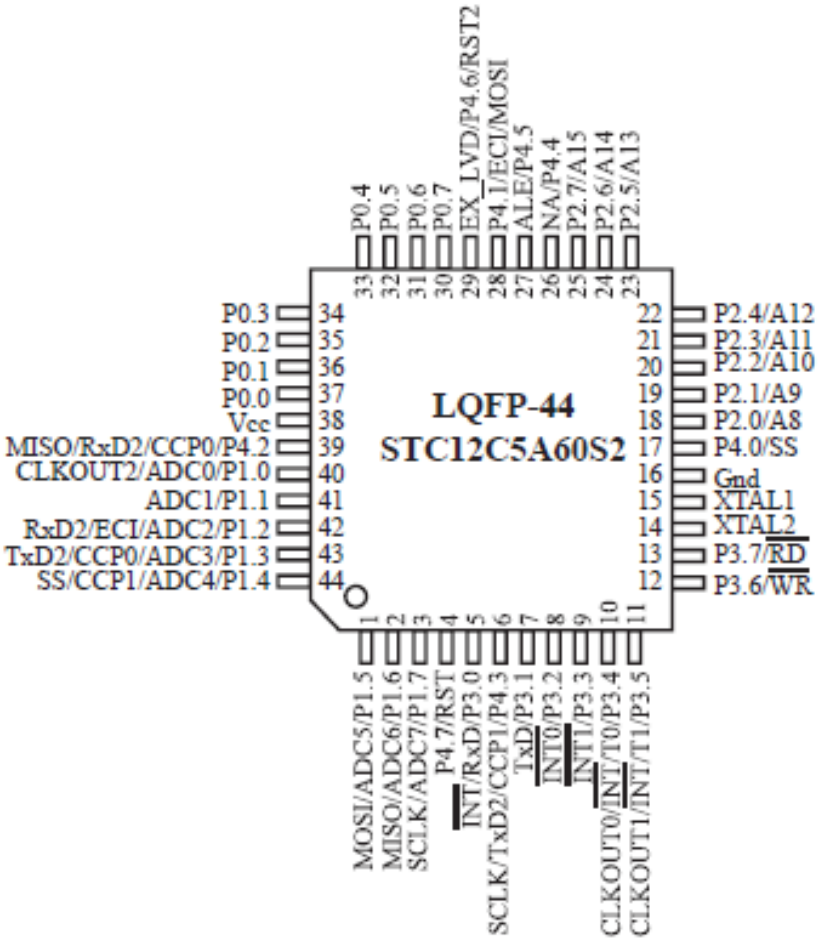
F8									FF
F0	**B**								F7
E8									EF
E0	**ACC**								E7
D8									DF
D0	**PSW**								D7
C8									CF
C0									C7
B8	**IP**								BF
B0	**P3**								B7
A8	**IE**								AF
A0	**P2**								A7
98	**SCON**	**SBUF**							9F
90	**P1**								97
88	**TCON**	**TMOD**	**TL0**	**TL1**	**TH0**	**TH1**			8F
80	**P0**	**SP**	**DPL**	**DPH**				**PCON**	87

STC12C5A60S2

STC12C5A60S2

- STC8051 family by STCmicro Technology
  - also produced stc32 8051 and stc32 ARM
- fully compatible 8051 instructions set
- many feature upgrades
  - low power consumption (3.3v also available)
  - higher speed (1T execution)
  - on-chip user code can be encrypted
  - on-chip ADC
  - more GPIO

STC12C5A60S2 Pin Diagram



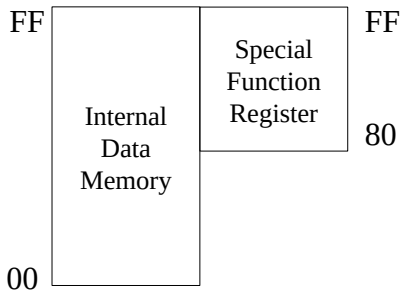
STC12C5A60S2 Architecture

STC12C5A60S2: Code Memory

- 60kB on-chip flash memory
  - no $\overline{\text{EA}}$ and $\overline{\text{PSEN}}$ pins for external code memory!

STC12C5A60S2: Data Memory

- 256-byte scratch-pad RAM
  - as in 8052 (additional 128 bytes)



- 1024-byte auxiliary RAM
  - access as external RAM
  - assembly access using movx instruction
  - c variables declared as xdata

STC12C5A60S2: SFR

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
0F8H		CH 0000,0000	CCAP0H 0000,0000	CCAP1H 0000,0000					0FFH
0F0H	B 0000,0000		PCA_PWM0 xxxx,xx00	PCA_PWM1 xxxx,xx00					0F7H
0E8H		CL 0000,0000	CCAP0L 0000,0000	CCAP1L 0000,0000					0EFH
0E0H	ACC 0000,0000								0E7H
0D8H	CCON 00xx,xx00	CMOD 0xxx,0000	CCAPM0 x000,0000	CCAPM1 x000,0000					0DFH
0D0H	PSW 0000,0000								0D7H
0C8H	P5 xxxx,1111	P5M1 xxxx,0000	P5M0 xxxx,0000			SPSTAT 00xx,xxxx	SPCTL 0000,0100	SPDAT 0000,0000	0CFH
0C0H	P4 1111,1111	WDT_CONTR 0x00,0000	IAP_DATA 1111,1111	IAP_ADDRH 0000,0000	IAP_ADDRL 0000,0000	IAP_CMD xxxx,xx00	IAP_TRIG xxxx,xxxx	IAP_CONTR 0000,x000	0C7H
0B8H	IP 0000,0000	SADEN 0000,0000		P4SW x000,xxxx	ADC_CONTR 0000,0000	ADC_RES 0000,0000	ADC_RESL 0000,0000		0BFH
0B0H	P3 1111,1111	P3M1 0000,0000	P3M0 0000,0000	P4M1 0000,0000	P4M0 0000,0000	IP2 xxxx,xx00	IP2H xxxx,xx00	IPH 0000,0000	0B7H
0A8H	IE 0000,0000	SADDR 0000,0000						IE2 xxxx,xx00	0AFH
0A0H	P2 11111111	BUS_SPEED xx10,x011	AUXR1 0000,0000					TEST_WDT don't use	0A7H
098H	SCON 0000,0000	SBUF xxxx,xxxx	S2CON 0000,0000	S2BUF xxxx,xxxx	BRT 0000,0000	P1ASF 0000,0000			09FH
090H	P1 1111,1111	P1M1 0000,0000	P1M0 0000,0000	P0M1 0000,0000	P0M0 0000,0000	P2M1 0000,0000	P2M0 0000,0000	CLK_DIV xxxx,x000	097H
088H	TCON 00000000	TMOD 00000000	TL0 0000,0000	TL1 0000,0000	TH0 0000,0000	TH1 0000,0000	AUXR 0000,0000	WAKE_CLKO 0000,0x00	08FH
080H	P0 1111,1111	SP 0000,0111	DPL 0000,0000	DPH 0000,0000				PCON 0011,0000	087H
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Bit Addressable

Non Bit Addressable

End of Lecture02