PGT104 – Digital Electronics

Part 4 – Combinational Logic Circuits

Disclaimer:
- Most of the contents (if not all) are extracted from resources available for Digital Fundamentals 10th Edition
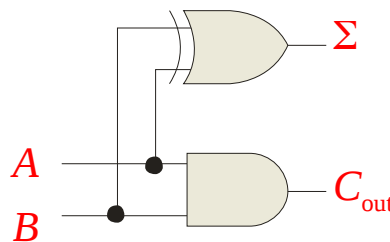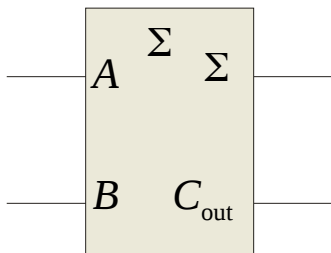
Half-Adder

Basic rules of binary addition are performed by a **half adder**, which has two binary inputs (A and B) and two binary outputs (Carry out and Sum).

The inputs and outputs can be summarized on a truth table.

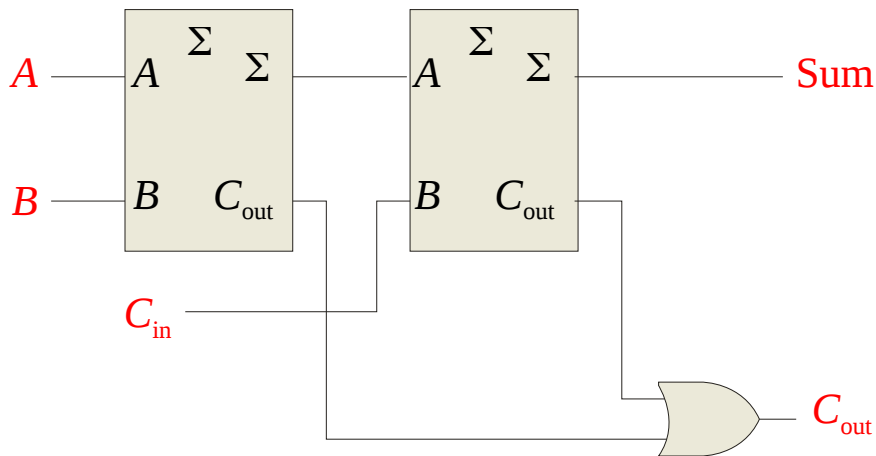| Inputs		Outputs	
A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

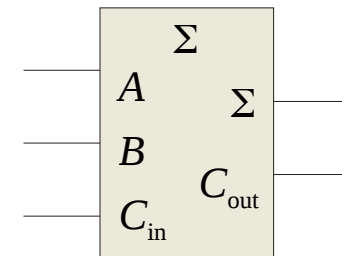The logic symbol and equivalent circuit are:

Full-Adder

By contrast, a **full adder** has three binary inputs (A, B, and Carry in) and two binary outputs (Carry out and Sum). The truth table summarizes the operation.

A full-adder can be constructed from two half adders as shown:

Inputs			Outputs	
A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

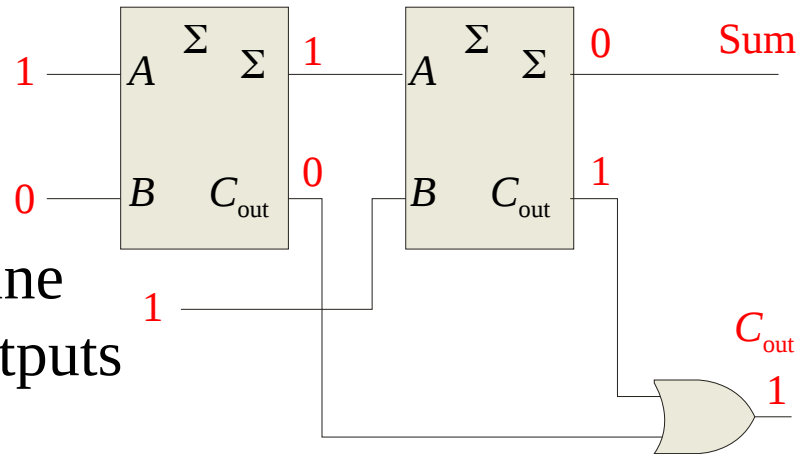
Symbol

Example

For the given inputs, determine the intermediate and final outputs of the full adder.

The first half-adder has inputs of 1 and 0; therefore the Sum =1 and the Carry out = 0.

The second half-adder has inputs of 1 and 1; therefore the Sum = 0 and the Carry out = 1.

The OR gate has inputs of 1 and 0, therefore the final carry out = 1.

Full-Adder

Notice that the result from the previous example can be read directly on the truth table for a full adder.

| Inputs			Outputs	
A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1
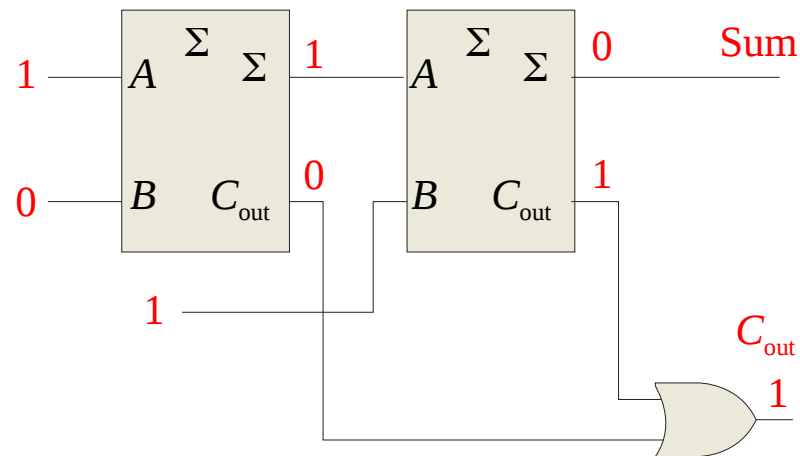
Parallel Adders

Full adders are combined into parallel adders that can add binary numbers with multiple bits. A 4-bit adder is shown.
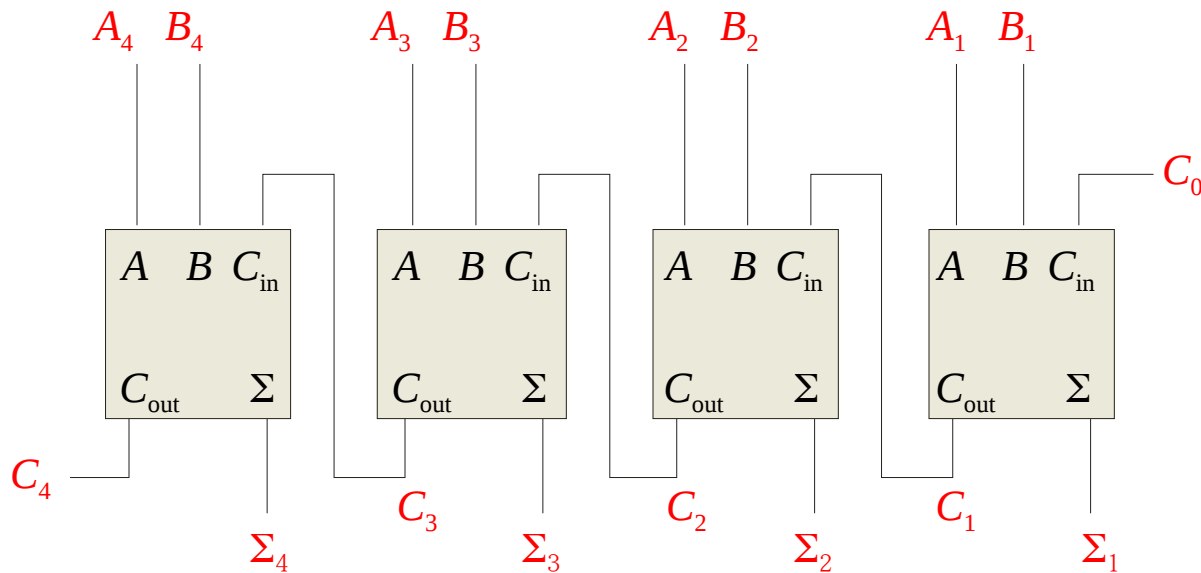
The output carry (C_4) is not ready until it propagates through all of the full adders. This is called *ripple carry*, delaying the addition process.

Parallel Adders

The logic symbol for a 4-bit parallel adder is shown. This 4-bit adder includes a carry in (labeled (C_0) and a Carry out (labeled C_4).
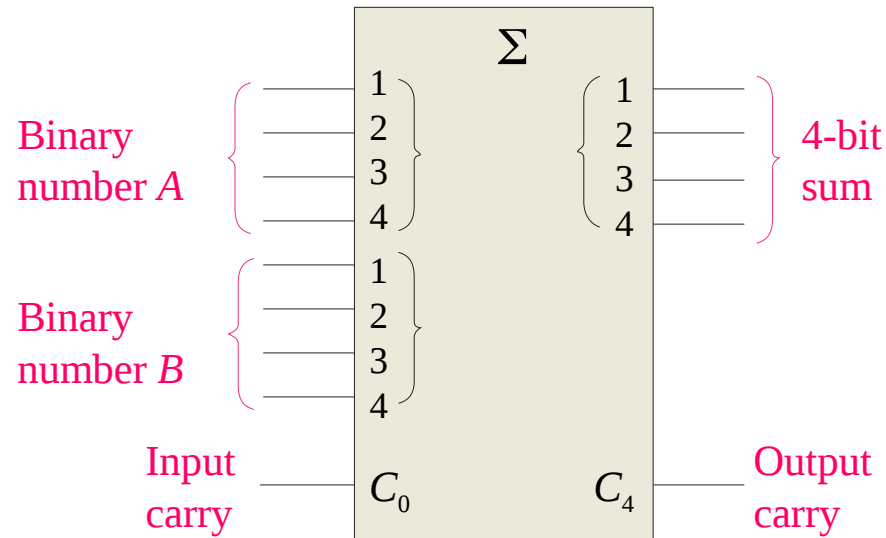
The 74LS283 is an example. It features *look-ahead carry*, which adds logic to minimize the output carry delay. For the 74LS283, the maximum delay to the output carry is 17 ns.
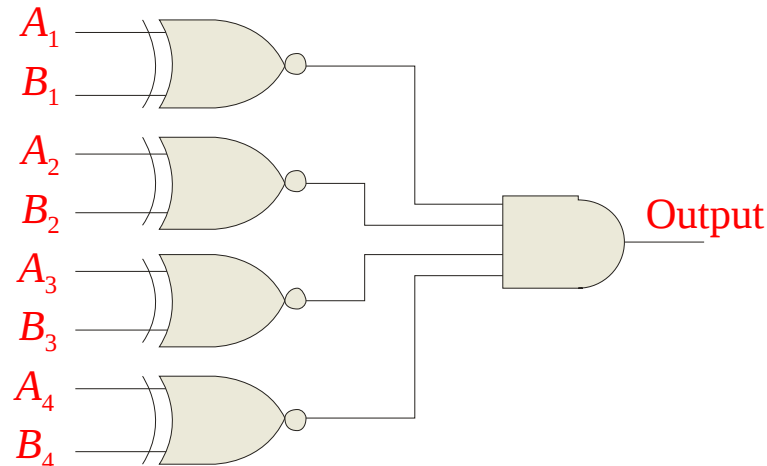
Comparators

The function of a comparator is to compare the magnitudes of two binary numbers to determine the relationship between them. In the simplest form, a comparator can test for equality using XNOR gates.
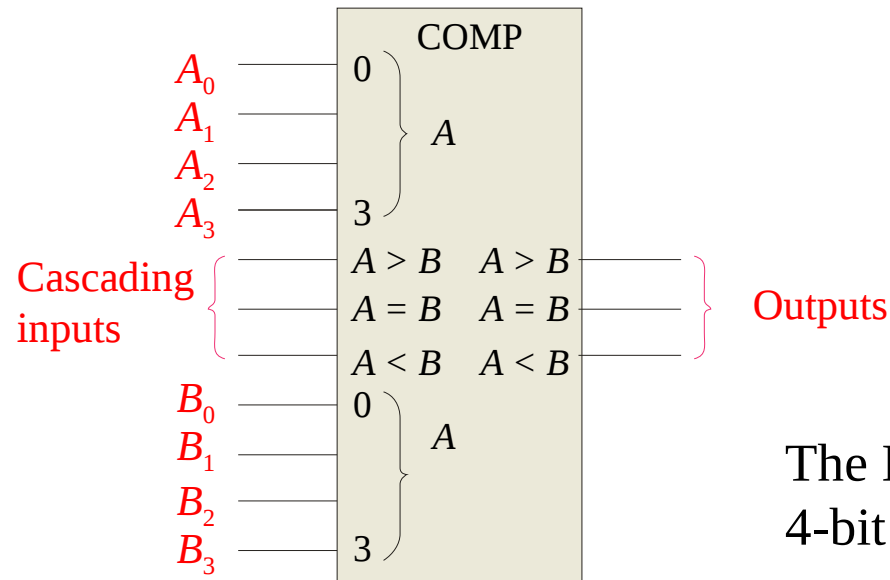
Example

How could you test two 4-bit numbers for equality?

AND the outputs of four XNOR gates.

Comparators

IC comparators provide outputs to indicate which of the numbers is larger or if they are equal. The bits are numbered starting at 0, rather than 1 as in the case of adders. Cascading inputs are provided to expand the comparator to larger numbers.

A_0 — 0   COMP

A_1 —

A_2 — A

A_3 — 3

Cascading inputs

$A > B$ $A > B$

$A = B$ $A = B$ Outputs

$A < B$ $A < B$

B_0 — 0

B_1 — A

B_2 —

B_3 — 3

The IC shown is the 4-bit 74LS85.

IC comparators can be expanded using the cascading inputs as shown. The lowest order comparator has a HIGH on the $A = B$ input.
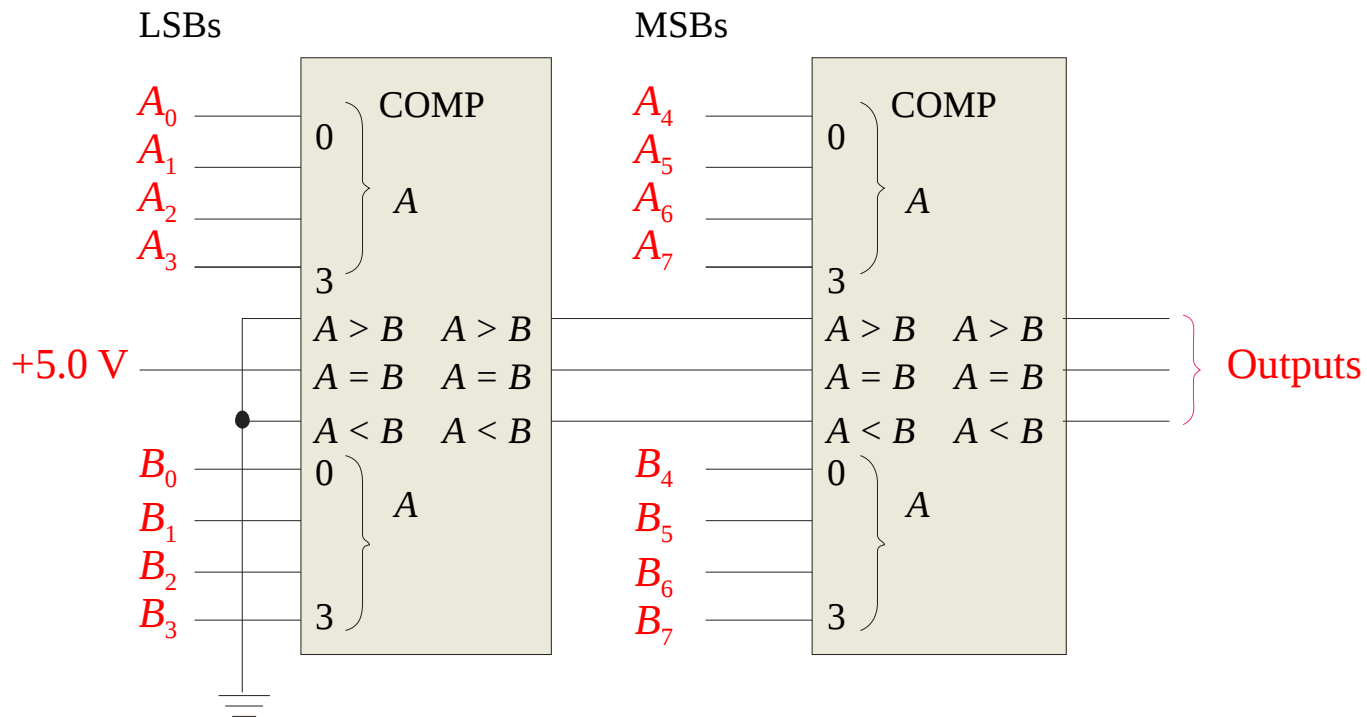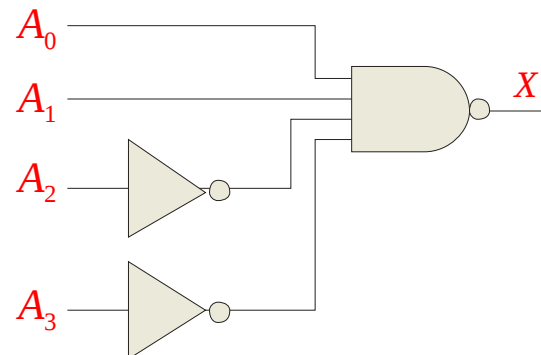
Decoders

A **decoder** is a logic circuit that detects the presence of a specific combination of bits at its input. Two simple decoders that detect the presence of the binary code 0011 are shown. The first has an active HIGH output; the second has an active LOW output.
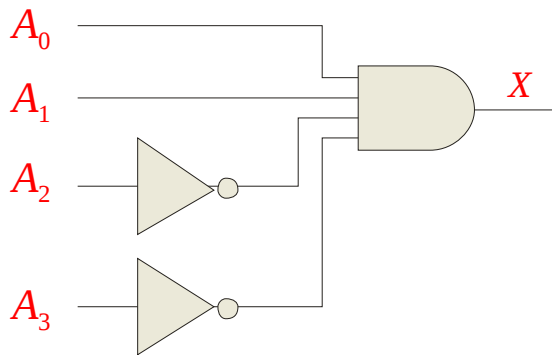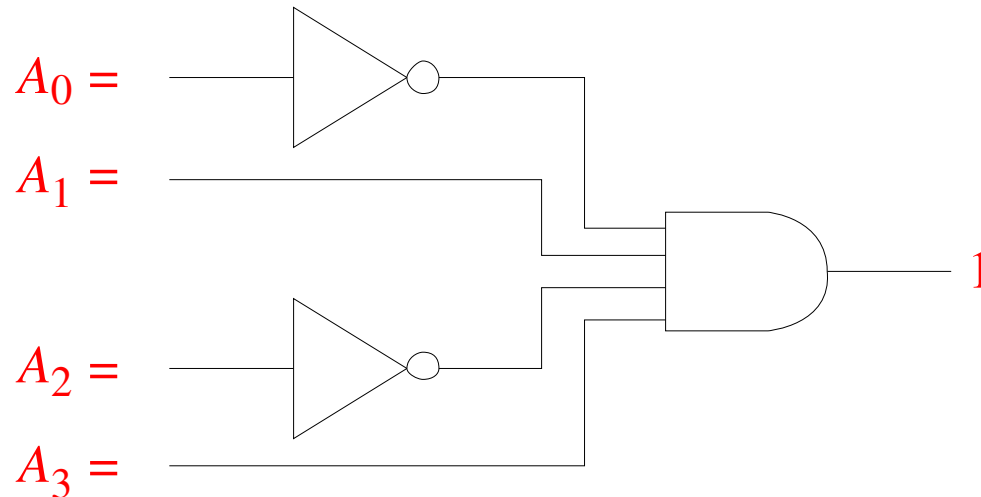

Active HIGH decoder for 0011

Active LOW decoder for 0011

Try This!

Assume the output of the decoder shown is a logic 1. What are the inputs to the decoder?

$A_0 =$

$A_1 =$

$A_2 =$

$A_3 =$

1

Decoders

IC decoders have multiple outputs to decode any combination of inputs. For example the binary-to-decimal decoder shown here has 16 outputs – one for each combination of binary inputs.

Try This!

For the input shown, what is the output?

Bin/Dec

0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

4-bit binary input

1 — A_0
1 — A_1
0 — A_2
1 — A_3

Decimal outputs

Decoders

A specific integrated circuit decoder is the 74HC154 (shown as a 4-to-16 decoder). It includes two active LOW chip select lines which must be at the active level to enable the outputs. These lines can be used to expand the decoder to larger inputs.


74HC154
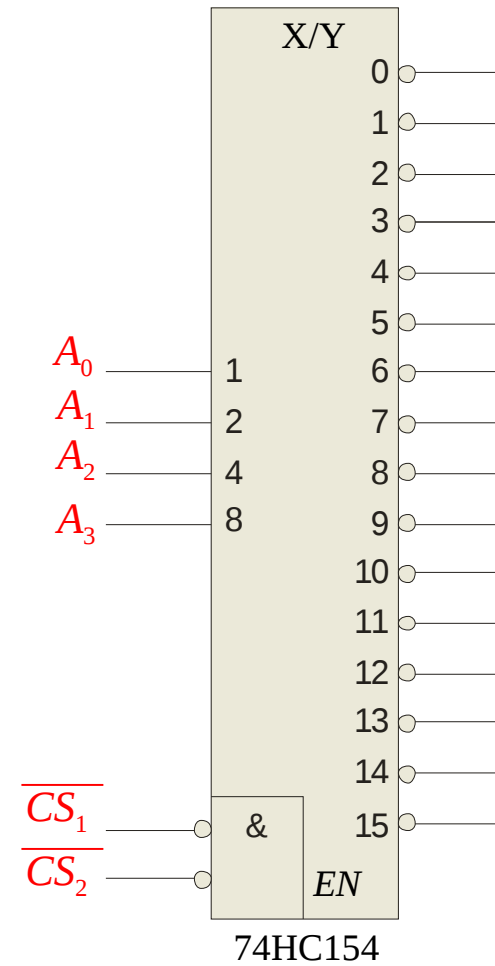
Checkpoint

- Another decoder IC is 74LS138
  - a 3-8 decoder (active low output)
  - 3 'enable' bits (G1 - active high, /G2A & /G2B – active low)

- Let a 3-bit counter (output $C_2C_1C_0$) to be used as input to a 74LS138 IC
  - assume all enable bits asserted
  - sketch the output if counter is counting up

Decoders

BCD-to-decimal decoders accept a binary coded decimal input and activate one of ten possible decimal digit indications.
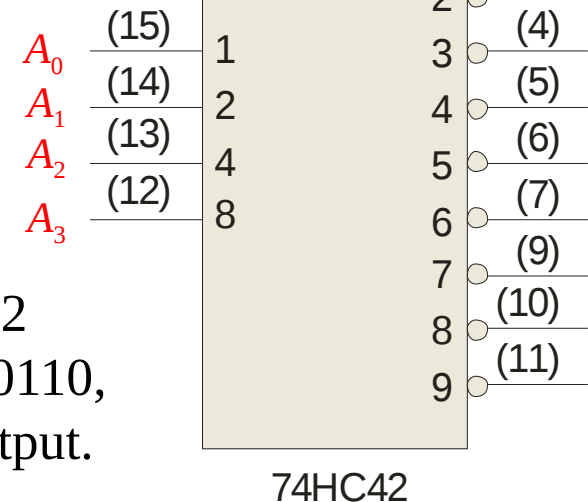
Example

Assume the inputs to the 74HC42 decoder are the sequence 0101, 0110, 0011, and 0010. Describe the output.

All lines are HIGH except for one active output, which is LOW. The active outputs are 5, 6, 3, and 2 in that order.

BCD/DEC

A_0 (15) — 1
A_1 (14) — 2
A_2 (13) — 4
A_3 (12) — 8

0 — (1)
1 — (2)
2 — (3)
3 — (4)
4 — (5)
5 — (6)
6 — (7)
7 — (9)
8 — (10)
9 — (11)

74HC42

BCD Decoder/Driver

Another useful decoder is the 74LS47. This is a BCD-to-seven segment display with active LOW outputs.

The *a-g* outputs are designed for much higher current than most devices (hence the word driver in the name).
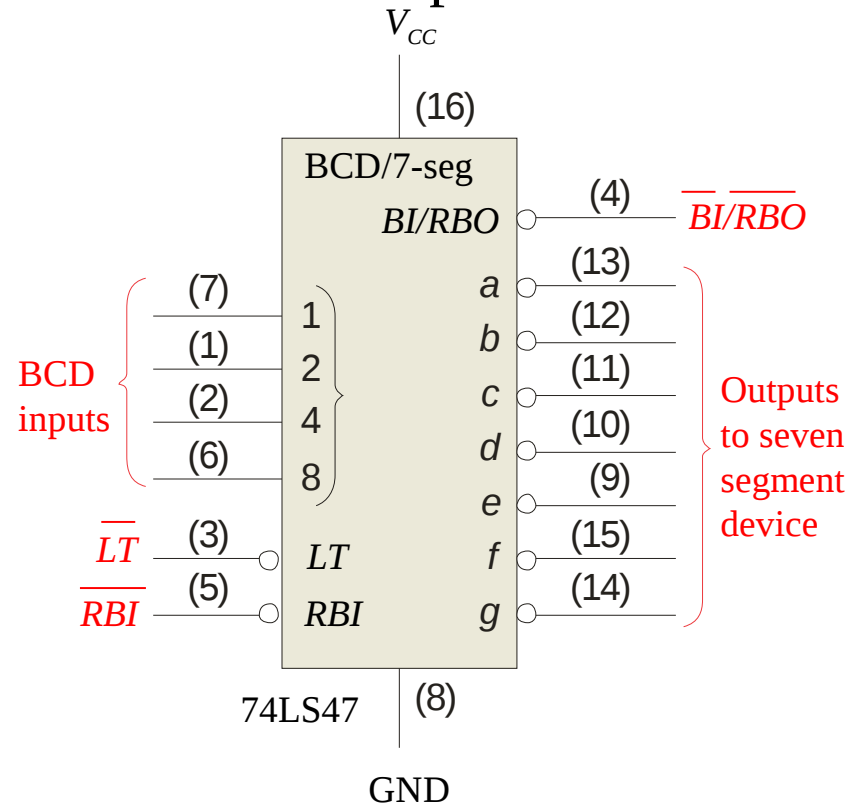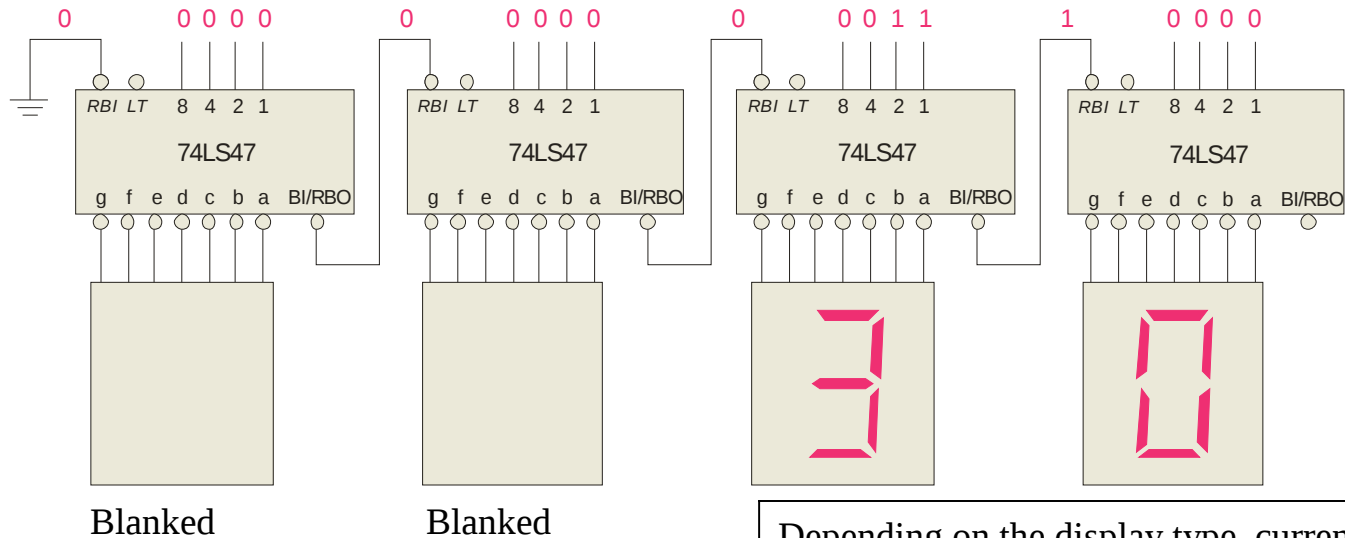
BCD Decoder/Driver

Here the 7447A is an connected to an LED seven segment display. Notice the current limiting resistors, required to prevent overdriving the LED display.
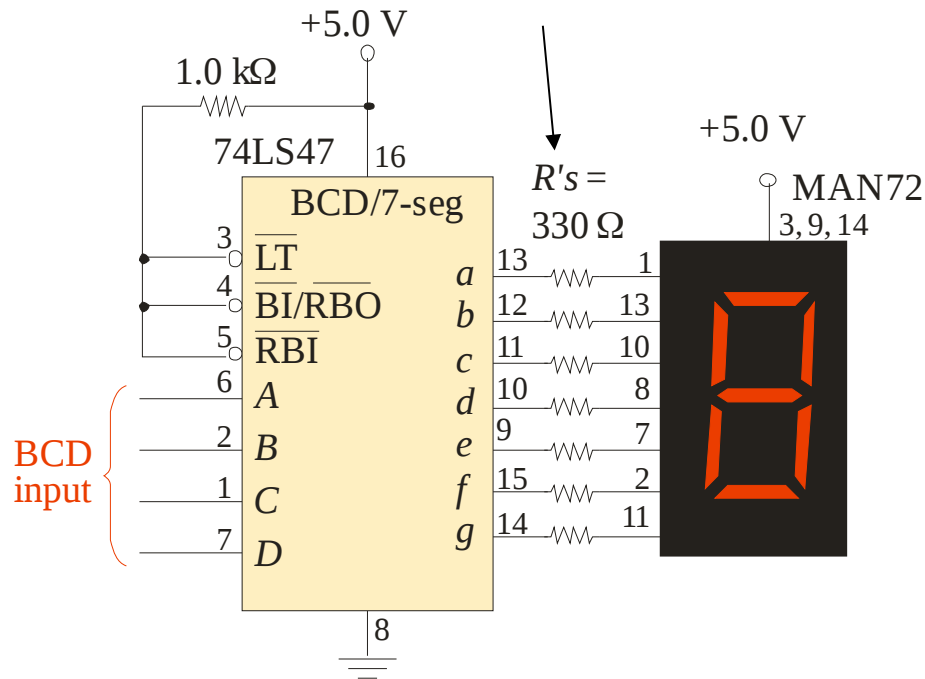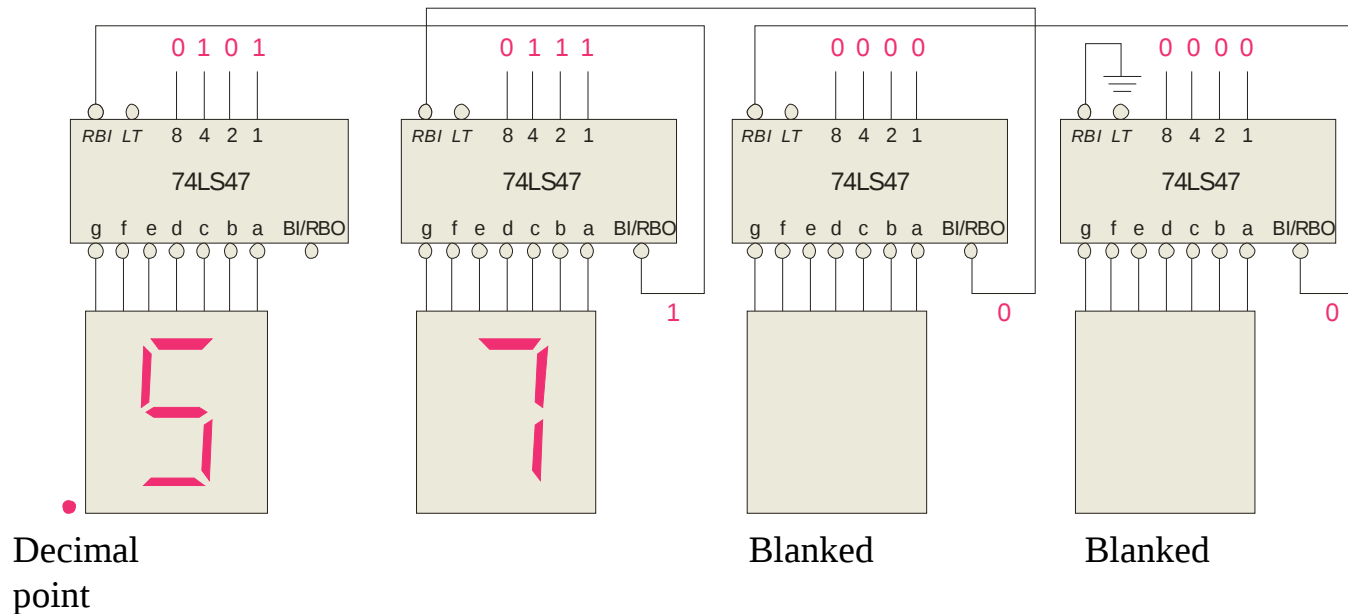
BCD Decoder/Driver

The 74LS47 features leading zero suppression, which blanks unnecessary leading zeros but keeps significant zeros as illustrated here. The *BI/RBO* output is connected to the *RBI* input of the next decoder.

Blanked   Blanked

Depending on the display type, current limiting resistors may be required.

Trailing zero suppression blanks unnecessary trailing zeros to the right of the decimal point as illustrated here. The *RBI* input is connected to the *BI/RBO* output of the following decoder.

0 1 0 1

| RBI LT | 8 4 2 1 |
| 74LS47 |
| g f e d c b a | BI/RBO |

0 1 1 1

| RBI LT | 8 4 2 1 |
| 74LS47 |
| g f e d c b a | BI/RBO |

1

0 0 0 0

| RBI LT | 8 4 2 1 |
| 74LS47 |
| g f e d c b a | BI/RBO |

0

0 0 0 0

| RBI LT | 8 4 2 1 |
| 74LS47 |
| g f e d c b a | BI/RBO |

0

Decimal point

Blanked

Blanked

An **encoder** accepts an active logic level on one of its inputs and converts it to a coded output, such as BCD or binary.

The decimal to BCD is an encoder with an input for each of the ten decimal digits and four outputs that represent the BCD code for the active digit. The basic logic diagram is shown. There is no zero input because the outputs are all LOW when the input is zero.
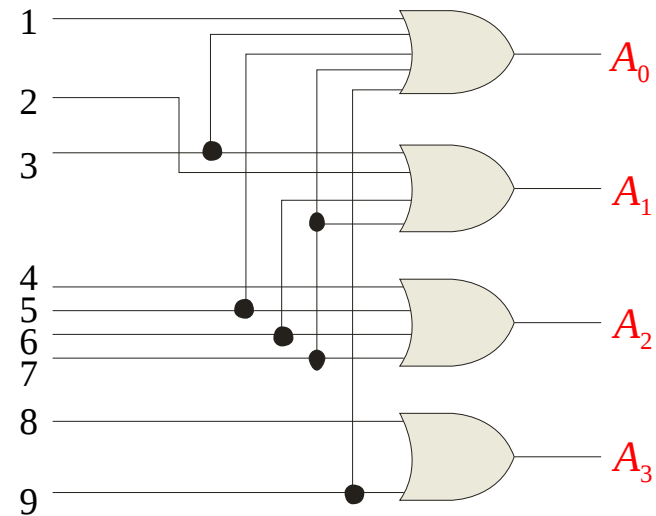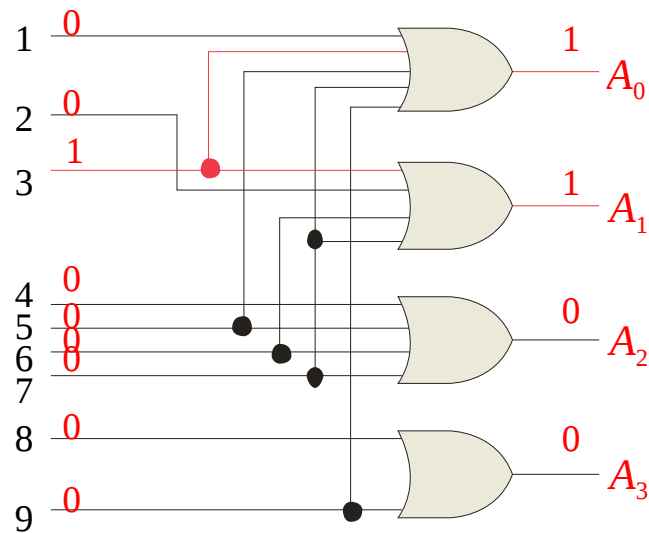
Encoders

Show how the decimal-to-BCD encoder converts the decimal number 3 into a BCD 0011.
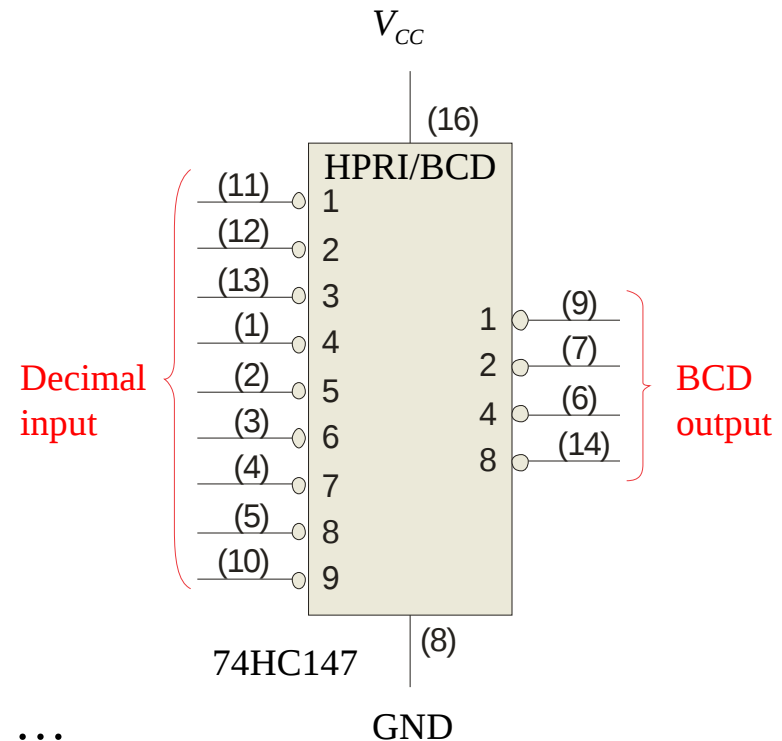
Example

The top two OR gates have ones as indicated with the red lines. Thus the output is 0111.

Encoders

The 74HC147 is an example of an IC encoder. It is has ten active-LOW inputs and converts the active input to an active-LOW BCD output.
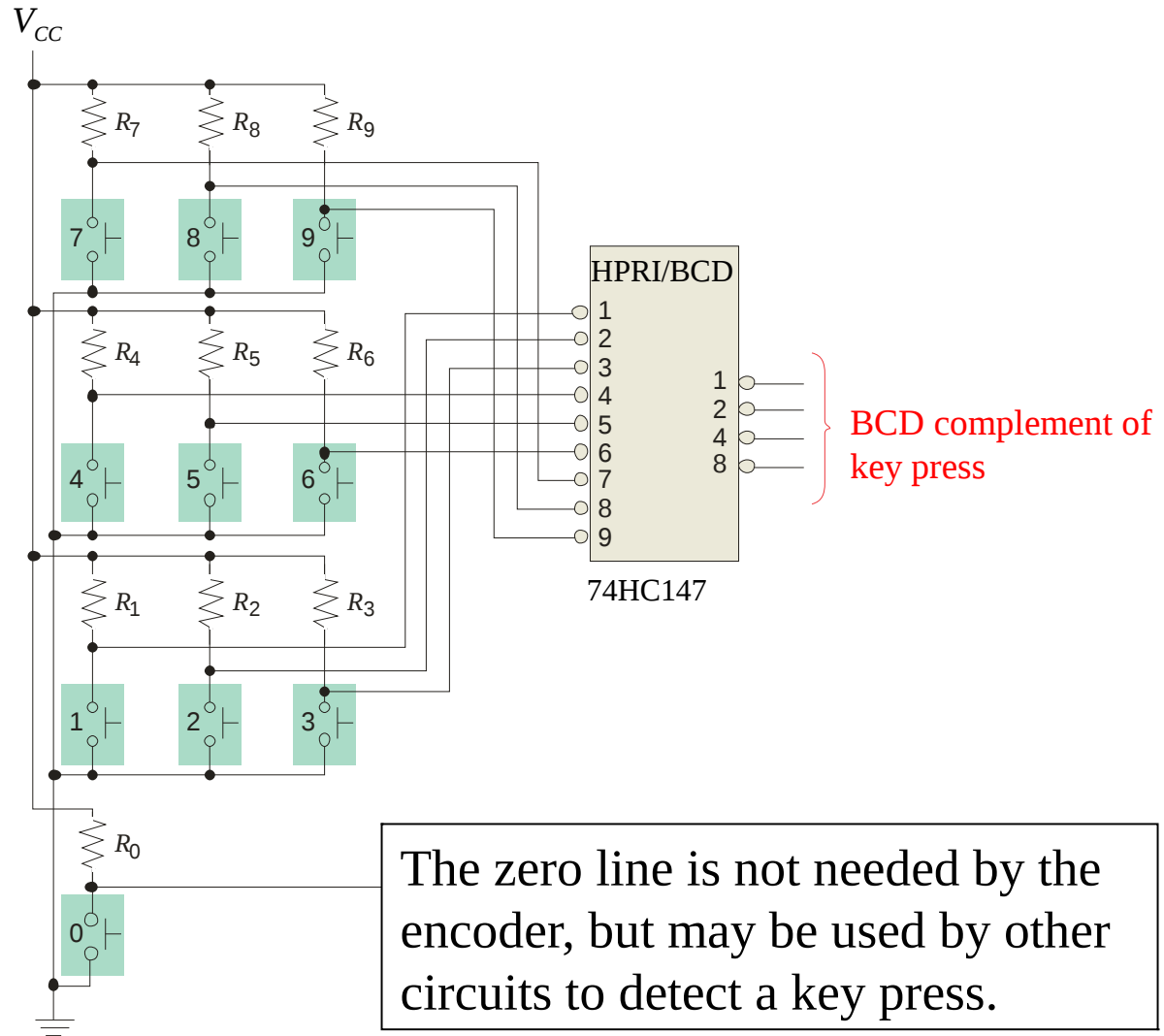
This device is offers additional flexibility in that it is a **priority encoder**. This means that if more than one input is active, the one with the highest order decimal digit will be active.

The next slide shows an application …

V_{CC}

HPRI/BCD

Decimal input

(11) 1
(12) 2
(13) 3
(1) 4
(2) 5
(3) 6
(4) 7
(5) 8
(10) 9

1 (9)
2 (7)
4 (6)
8 (14)

BCD output

(16)

(8)

74HC147

GND

Encoders

Keyboard encoder

BCD complement of key press

The zero line is not needed by the encoder, but may be used by other circuits to detect a key press.

Checkpoint

- Gray code (reflected binary code)
  - only 1 bit changes between 2 successive value
 - very useful for error detection/correction

2-bit Gray Code	3-bit Gray Code
00	000
01	001
11	011
10	010
	110
	111
	101
	100

Code converters

There are various code converters that change one code to another. Two examples are the four bit binary-to-Gray converter and the Gray-to-binary converter.

Show the conversion of binary 0111 to Gray and back.

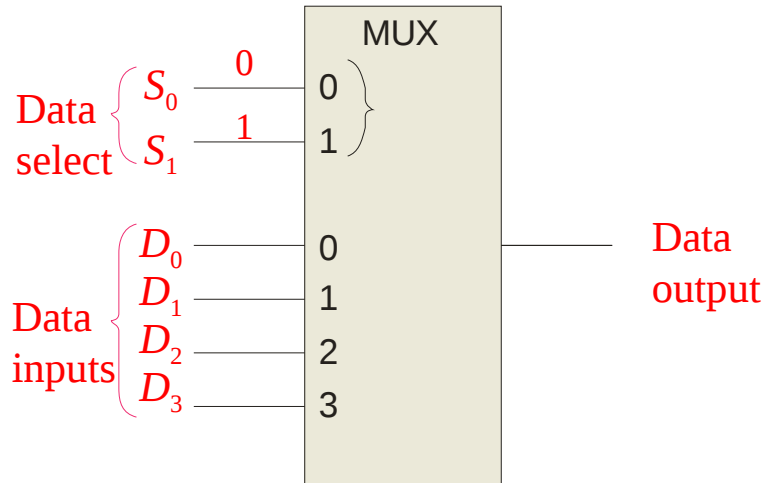Try This!

Binary-to-Gray

Gray-to-Binary
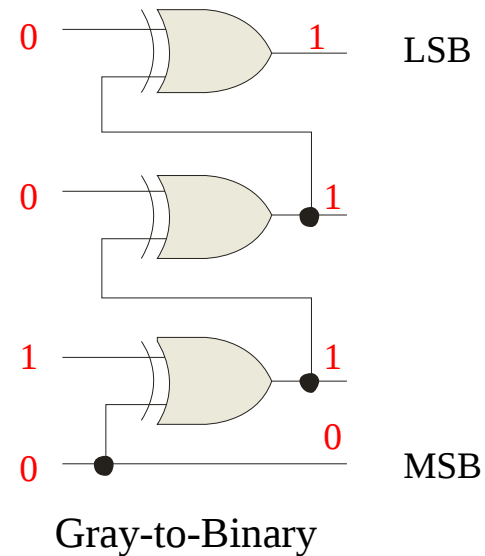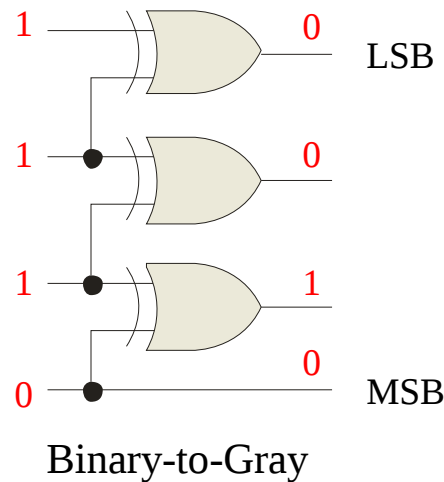
Multiplexers

A multiplexer (MUX) selects one data line from two or more input lines and routes data from the selected line to the output. The particular data line that is selected is determined by the select inputs.

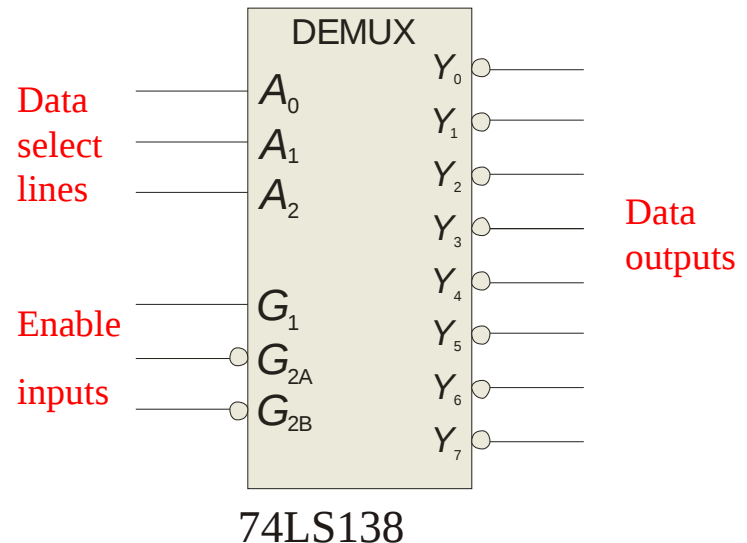Two select lines are shown here to choose any of the four data inputs.

Try This!

Which data line is selected if $S_1S_0 = 10$?

Demultiplexers

A demultiplexer (DEMUX) performs the opposite function from a MUX. It switches data from one input line to two or more data lines depending on the select inputs.

The 74LS138 was introduced previously as a decoder but can also serve as a DEMUX. When connected as a DEMUX, data is applied to one of the enable inputs, and routed to the selected output line depending on the select variables. Note that the outputs are active-LOW as illustrated in the following example…
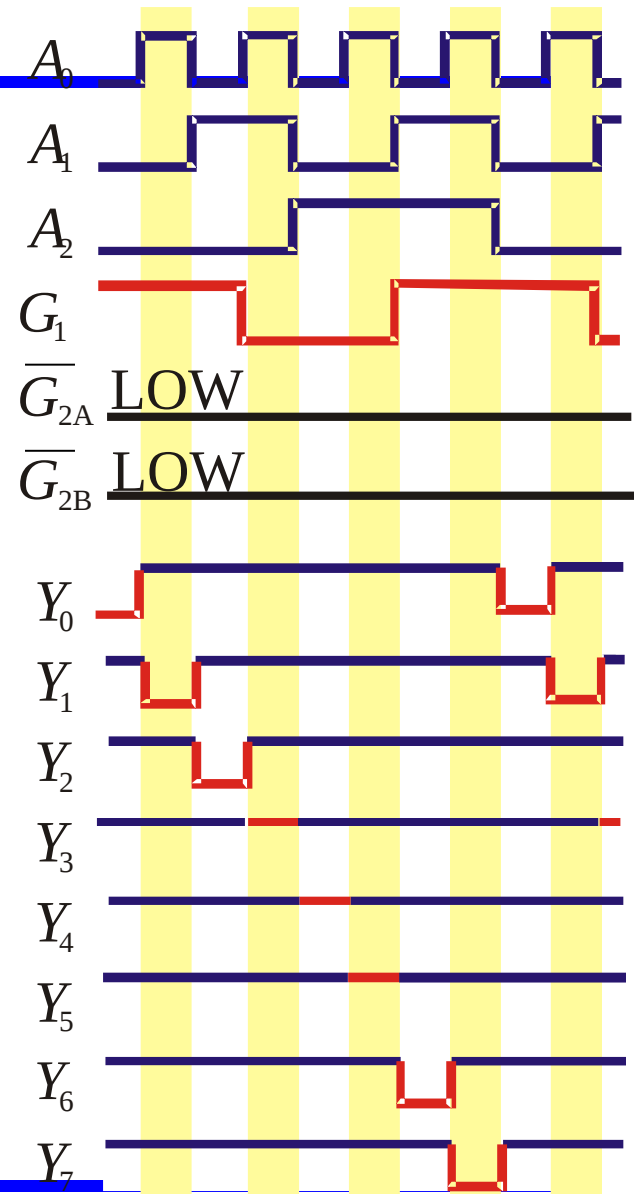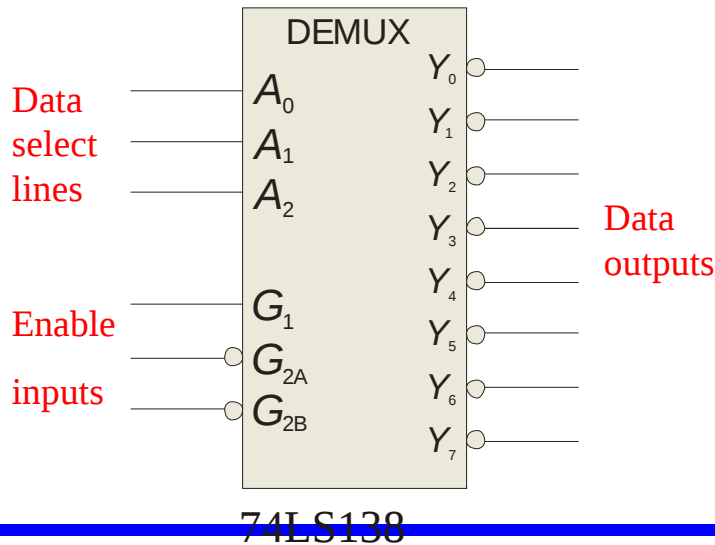
DEMUX

Data select lines → A_0, A_1, A_2

Enable inputs → G_1, G_{2A}, G_{2B}

Data outputs → Y_0, Y_1, Y_2, Y_3, Y_4, Y_5, Y_6, Y_7

74LS138

Demultiplexers

Determine the outputs, given the inputs shown.

Try This!

The output logic is opposite to the input because of the active-LOW convention. (Red shows the selected line).

```
              DEMUX
Data        A₀        Y₀
select      A₁        Y₁
lines       A₂        Y₂
                      Y₃      Data
                      Y₄      outputs
            G₁        Y₅
Enable    ○ G₂ₐ       Y₆
inputs    ○ G₂ᵦ       Y₇
              74LS138
```

A_0
A_1
A_2
G_1
$\overline{G}_{2A}$ LOW
$\overline{G}_{2B}$ LOW
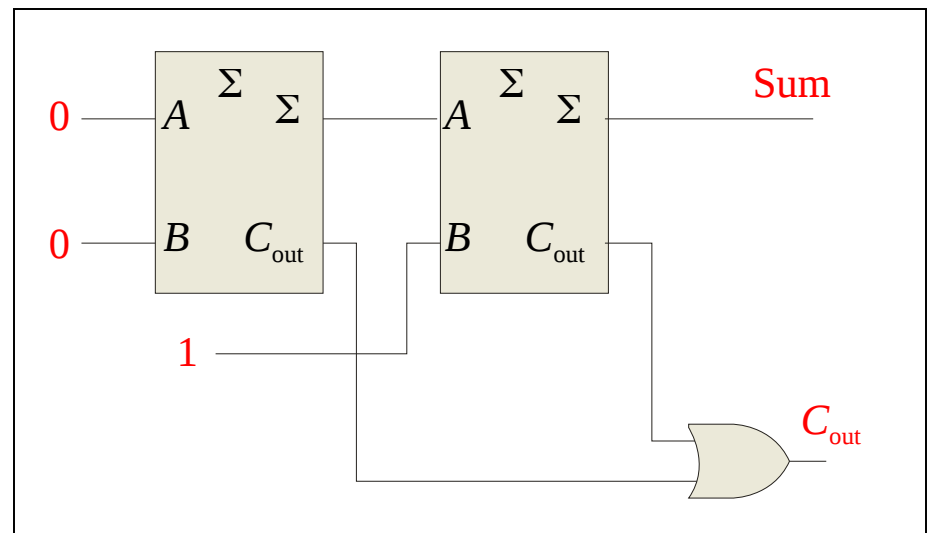
Y_0
Y_1
Y_2
Y_3
Y_4
Y_5
Y_6
Y_7

Quiz

For the full-adder shown, assume the input bits are as shown with $A = 0$, $B = 0$, $C_{in} = 1$. The Sum and C_{out} will be

a. Sum = 0 C_{out} = 0

b. Sum = 0 C_{out} = 1

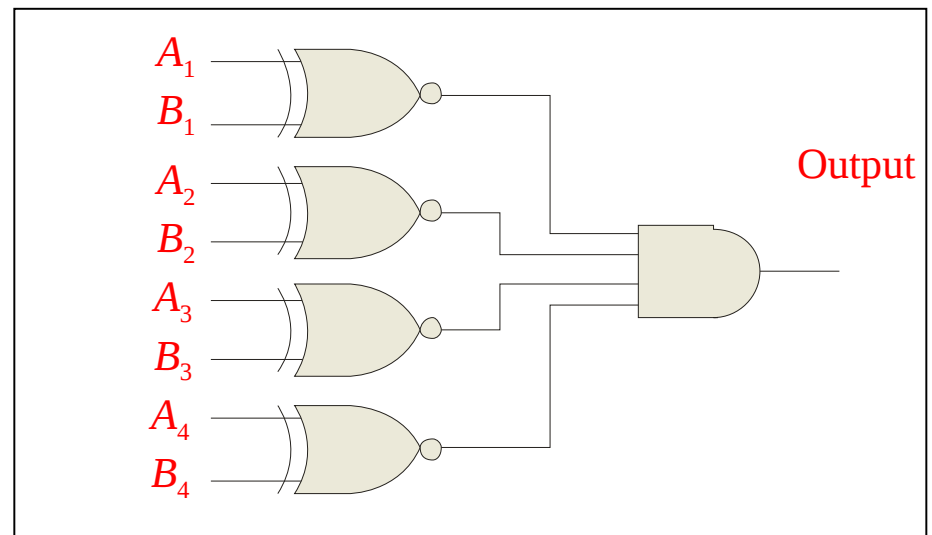c. Sum = 1 C_{out} = 0

d. Sum = 1 C_{out} = 1

Quiz

The output will be LOW if

    a. $A < B$

    b. $A > B$

    c. both a and b are
   correct

    d. $A = B$

Quiz

If you expand two 4-bit comparators to accept two 8-bit numbers, the output of the least significant comparator is

     a. equal to the final output

     b. connected to the cascading inputs of the most significant comparator

     c. connected to the output of the most significant comparator

     d. not used

Quiz

Assume you want to decode the binary number 0011 with an active-LOW decoder. The missing gate should be
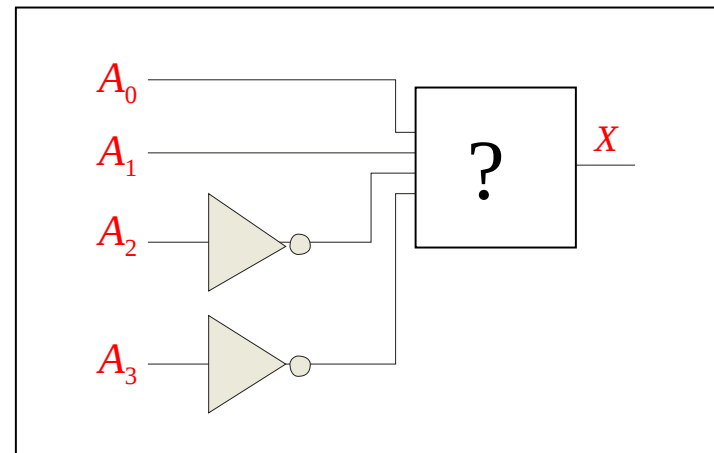
a. an AND gate

b. an OR gate

c. a NAND gate
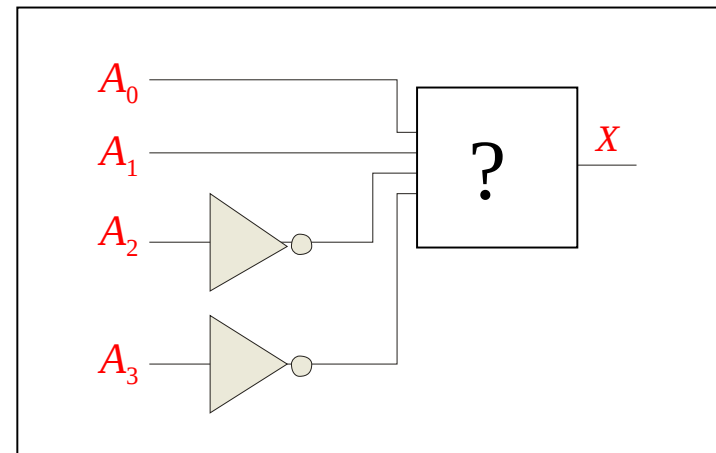
d. a NOR gate

Quiz

Assume you want to decode the binary number 0011 with an active-HIGH decoder. The missing gate should be

a. an AND gate

b. an OR gate

c. a NAND gate

d. a NOR gate

Quiz

The 74138 is a 3-to-8 decoder. Together, two of these ICs can be used to form one 4-to-16 decoder. To do this, connect

a. one decoder to the LSBs of the input; the other decoder to the MSBs of the input

b. all chip select lines to ground

c. all chip select lines to their active levels

d. one chip select line on each decoder to the input MSB

Quiz

The decimal-to-binary encoder shown does not have a zero input. This is because
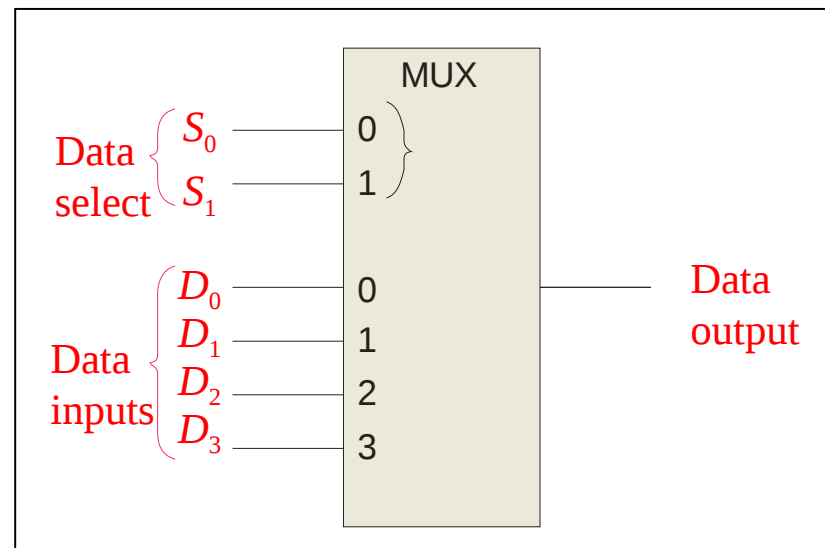
    a. when zero is the input, all lines should be LOW

    b. zero is not important

    c. zero will produce illegal logic levels

    d. another encoder is used for zero
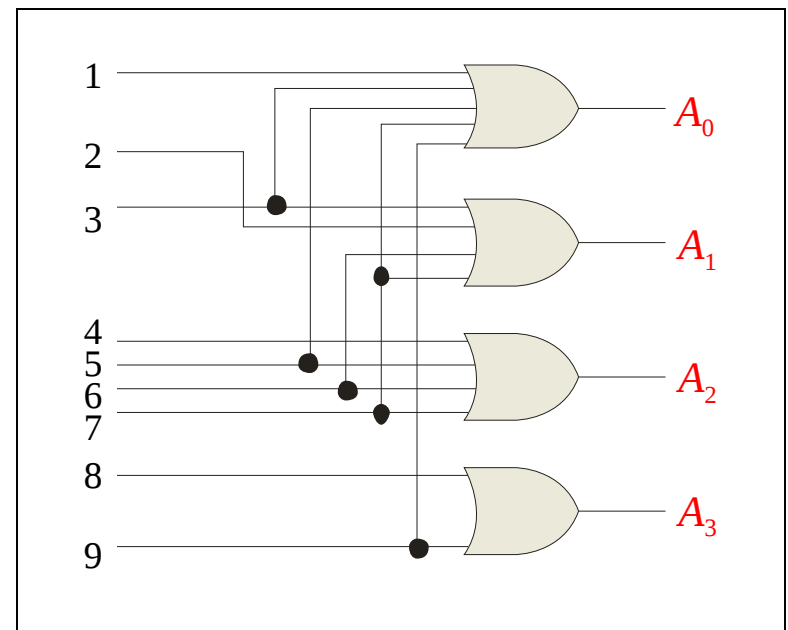
Quiz

If the data select lines of the MUX are $S_1S_0 = 11$, the output will be

a. LOW

b. HIGH

c. equal to D_0

d. equal to D_3

Quiz

The 74138 decoder can also be used as

a. an encoder

b. a DEMUX

c. a MUX

d. none of the above