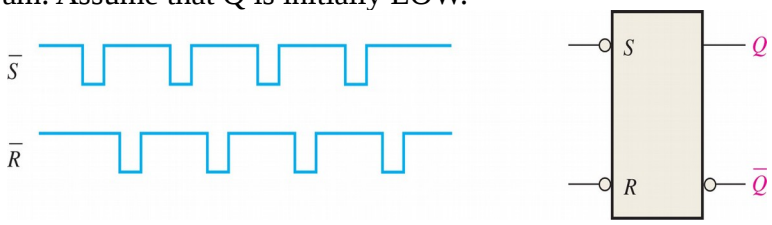
PGT104 – Assignment 2

Name: _____

Student ID: _____ Program: _____

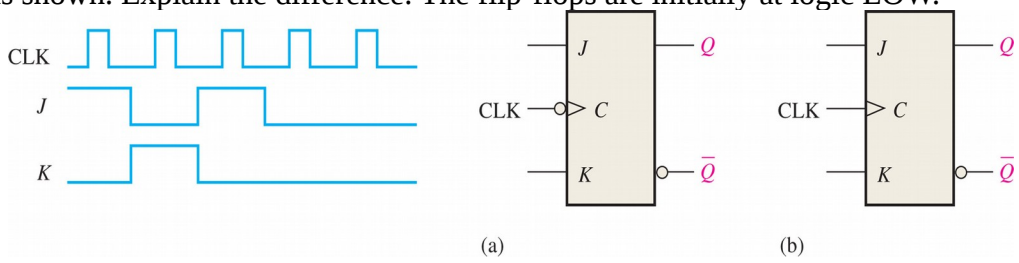
Answer all questions.

1. For an active-LOW $\overline{S}$-$\overline{R}$ latch, determine Q and $\overline{Q}$ outputs for inputs in figure below. Show them in a proper timing diagram. Assume that Q is initially LOW.



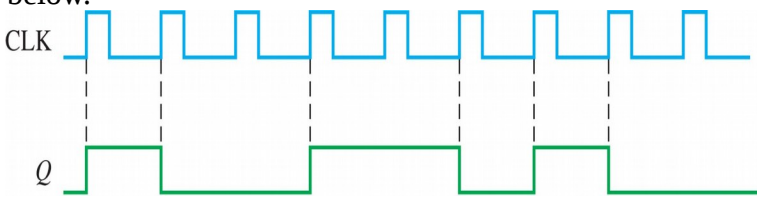
[8 marks]

2. For the two edge-triggered J-K flip-flops shown below, draw the Q output of each flip-flop if the inputs are as shown. Explain the difference. The flip-flops are initially at logic LOW.



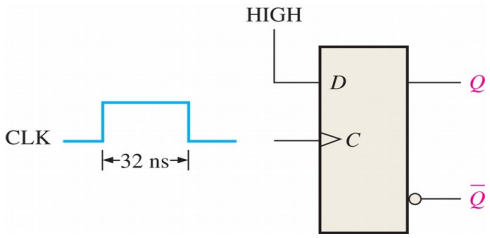
[12 marks]

3. For a positive edge-triggered D flip-flop, determine the input D waveform that is required to produce the Q output shown below.



[10 marks]

4. The D flip-flop in figure below is initially at logic LOW. Show the detail relationship (with time reference) between Q output and the given clock pulse (32 ns) if propagation delays are given as t_{PLH} = 5 ns and t_{PHL} = 4 ns.



[10 marks]

5. Find a suitable application for a one-shot device built using 555 timer. Draw a block diagram to show how the one-shot circuit is connected to the system. With a practical pulse-width value, calculate a practical/logical values for any passive components (R or L or C) required. Your answer should not be more than 1 page, and will be given a zero if there is a duplicate answer.

[10 marks]