NMK20603

Computer Architecture

MY1

Codes so far:

- ✔ alu_4b

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Homework?

⇒ zbuff (>1b)

⇒ decode38

⇒ cmp_2b

Digital systems:

- combinational

  ⇒ logic gates (and/or/inv)

- sequential

  = latch/flip-flop

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Let's go sequential

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Describing Sequential Logic

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Latches & Flip-flop

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Difference?

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Trigger:

Level vs Edge!

Keyword

- always

⇒ like initial

```
always
begin
// code goes here
// data type: reg
// 'always' triggered
end
```

Syntax

- @()

⇒ sensitivity list

⇒ v95: or separated

⇒ v2k1: comma separated

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```
always @(A or B)
begin
// triggered when
// A/B changes
end
```

D Flip-flop

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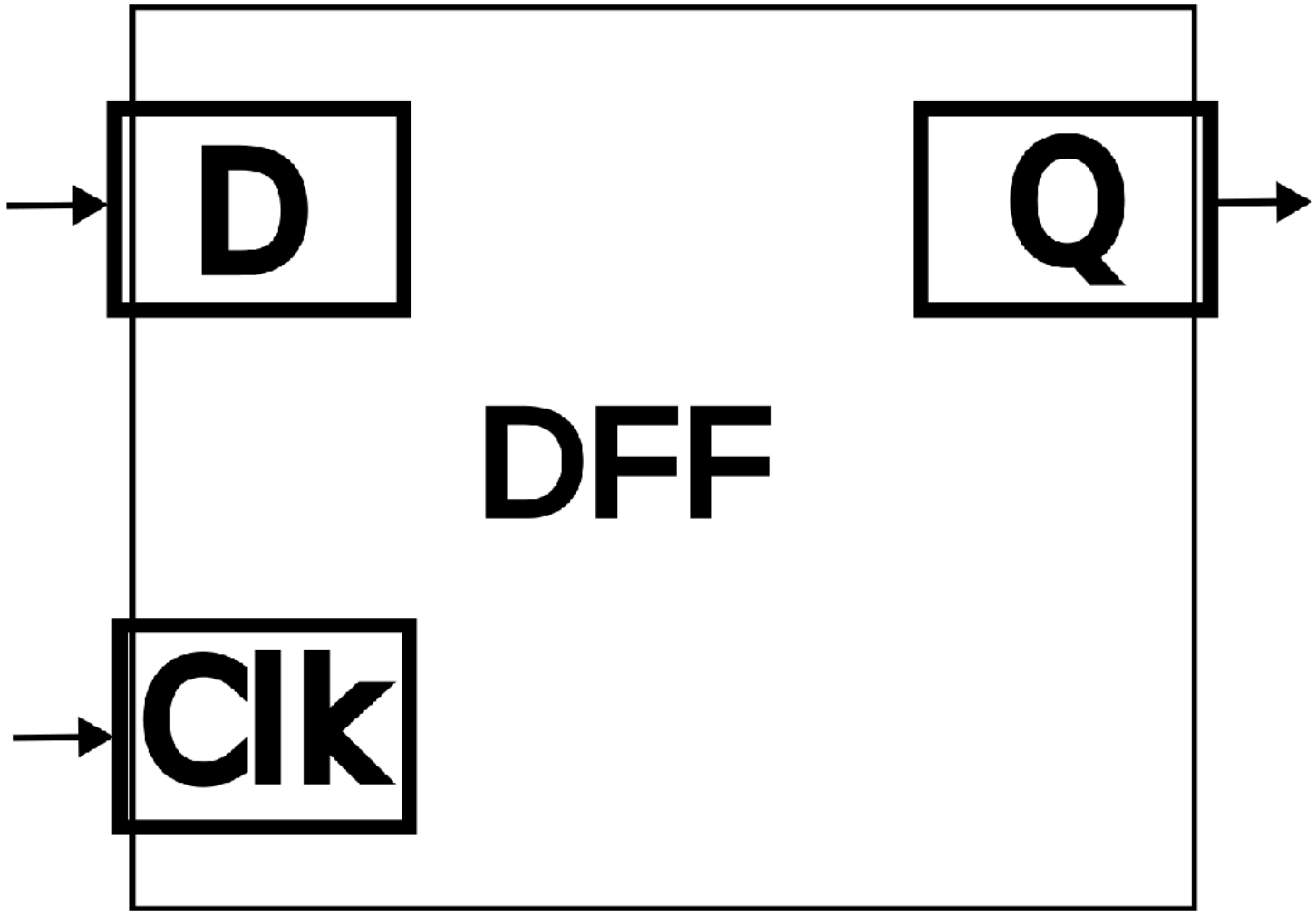
D
Q
DFF
Clk

Describe:

dff

```
module dff (iclk,idat,odat);
input iclk,idat;
output odat;
reg odat;
always @(iclk) begin
  if (iclk==1'b1) begin
    odat = idat;
  end
end
endmodule
```

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Syntax

- reg assignment

⇒ = vs <=

⇒ sequence vs concurrent

```
always @(idat) begin
   tdat = idat
   odat = tdat;
   // odat always same as tdat
end
```

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```
always @(idat) begin
   tdat <= idat
   odat <= tdat;
   // odat may differ from tdat
end
```

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Testbench?

⇒ no 'template'

Clock 'generator'

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```
// use in tb
// 10TU clock period
parameter CLKP = 10;
reg dclk; // clock net
always begin
  #(CLKP/2) dclk = ~dclk;
end
```

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User task

@custom sequence!

Keyword

- task/endtask

⇒ for tb only

```
// assume @+ve edge dff
// assume driver net is ddat
// should call this @-ve edge
reg ddat;
task dff_wr ;
  input integer dbit;
  begin
    ddat = dbit;
    $display("-- [%g] WR-dff:'%b' ",$time,ddat);
    #(CLKP/2); // setup time
    // should latch here
    #(CLKP/2); // hold time
    // 1-cycle
  end
endtask
```

DFF output 'monitor'

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```
// detect dff output
// can also use mdat!
always @(dut.odat) begin
  $write("[%05g] dffQ=%b\n",$time,dut.odat);
end
```

Notice:

- dut.odat?

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Describe:

dff_tb

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```
module dff_tb ();
// clock generator
// task to write to dff
// dff output monitor
wire mdat;
// reset condition
initial begin
  dclk = 1'b1; //at tu=0, dclk is 1
  ddat = 1'b0;
  #(CLKP/2); // wait for -ve edge
  dff_wr(1);
  #CLKP;
  // verify here?
  #CLKP;
  dff_wr(0);
  #(CLKP*5);
  $stop;
end
dff dut (dclk,ddat,mdat);
endmodule
```

Register?

- dff with purpose!

⇒ wr/rd on request

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Ports:

- ✔ iclk, idat, odat
- ✔ wenb, renb (write/read enable)

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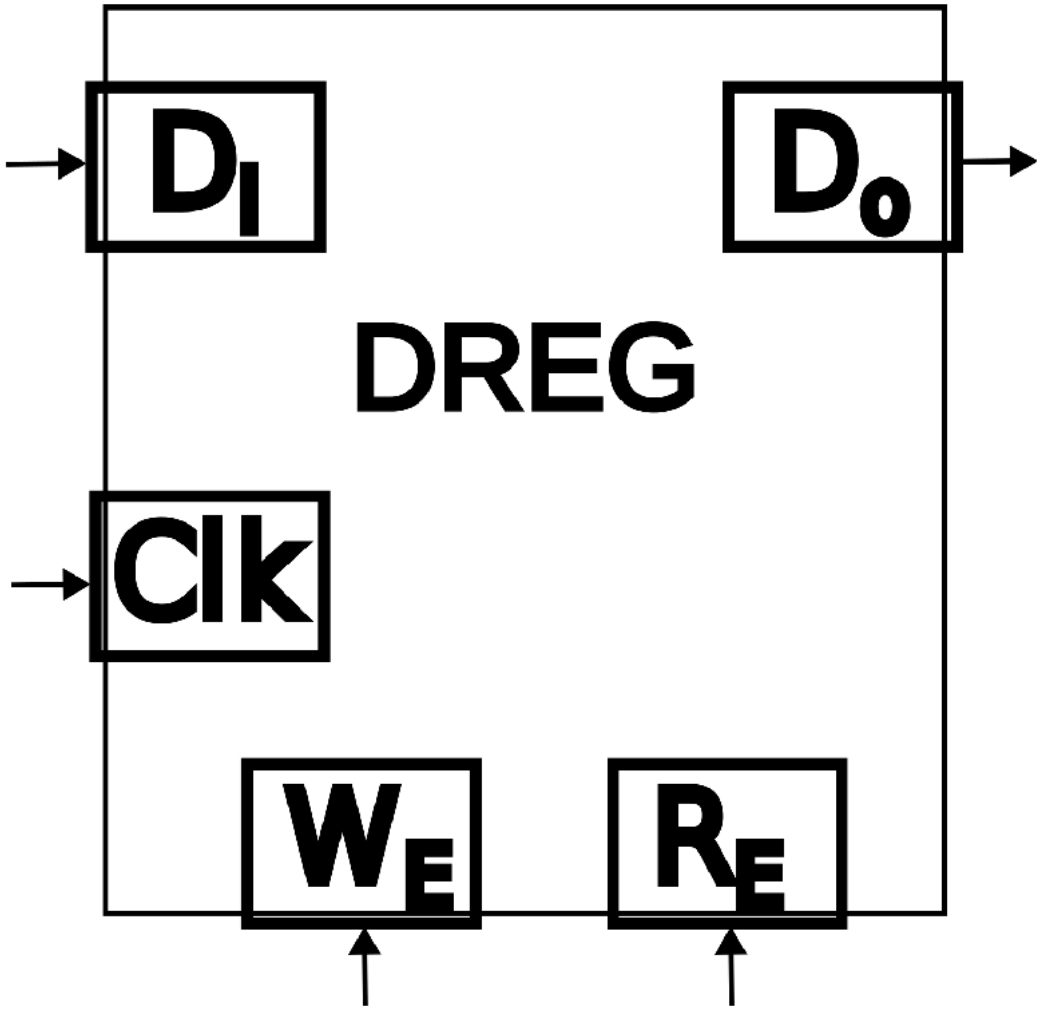
Syntax

- posedge

⇒ sensitivity list

```
always @(posedge dclk)
begin
// triggered when
// dclk transition 0->1
end
```



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Describe:

dreg

⇒ BITS=4

```
module dreg (iclk,wenb,renb,idat,odat);
parameter BITS=4;
input iclk,wenb,renb;
input[BITS-1:0] idat;
output[BITS-1:0] odat;
wire[BITS-1:0] odat
output[BITS-1:0] tdat;
always @(posedge iclk) begin
  if (wenb==1'b1) begin
    odat = idat;
  end
end
defparam oenb.BITS = BITS;
zbuff oenb (renb,tdat,odat);
endmodule
```

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Practice:

⇒ task>dreg_write

Practice:

⇒ task>dreg_read

Practice:

⇒ 'monitor' code for dreg?

Practice:

dreg_tb

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Register block?

- 4x4b register
- with bus to move!

⇒ what else do we need?

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Homework:

⇒ regblock4