NMK20603

Computer Architecture

MY1

Codes so far:

- ✔ alu_4b
- ✔ regblock4
- ✔ ringctr4

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Describing Simple Digital System

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State Machine incomplete...

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State/Sequence:

⇒ S1: get code

⇒ S2: read reg

⇒ S3: process

⇒ S4: write reg

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Completing Output

(@Control) Logic

✔ rs1_enb,rs2_enb, rd0_enb

✔ rs1_add,rs2_add, rd0_add

✔ alu_sel

⇒ 'hidden' lines

Processor Core

(Top level)

✔ 4b processor

⇒ @4b data bus

✔ 4 x 4b registers

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Input Logic?

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Instruction!

✔ sizeof inst

⇒ sizeof bus

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Let's do 8!

Instruction Set Architecture (ISA)

✔ register move

⇒ 1+2 params @ info

✔ alu operation

⇒ 1+3 params

✔ register load...

⇒ 1+2 params

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ISA design

- ✔ bits for inst id
- ✔ bits for param1
- ✔ bits for param2
- ✔ bits for param3

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Completing State Machine (and core!)

Note:

✔ state transition @-ve clk

⇒ dffepc write @+ve clk

✔ dreg @regblock write @+ve clk

⇒ dual clock? inv!

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Describe:

upcore

- ✔ iclk,irst,ienb,inst
- ✔ ostt,done

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Testbench?

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Describe: upcore_tb

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