Introduction to Verilog and ModelSim

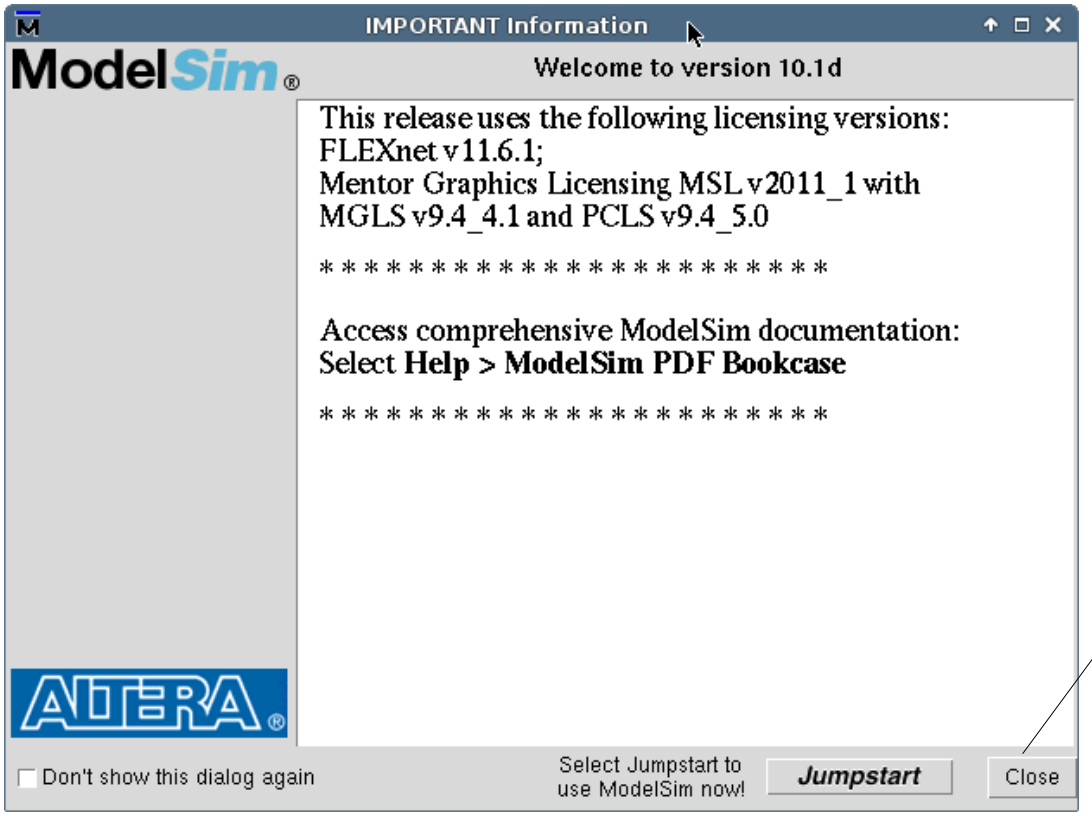
(Part 3 – Using ModelSim)

HDL Simulator

- ModelSim
  - Widely used in the industry
  - Can simulate either/both VHDL or/and Verilog
  - Has GUI interface (editor, waveform viewer)
- Alternative: Icarus Verilog
  - Open source simulation tool
  - Purely a Verilog simulator
  - Requires separate waveform viewer

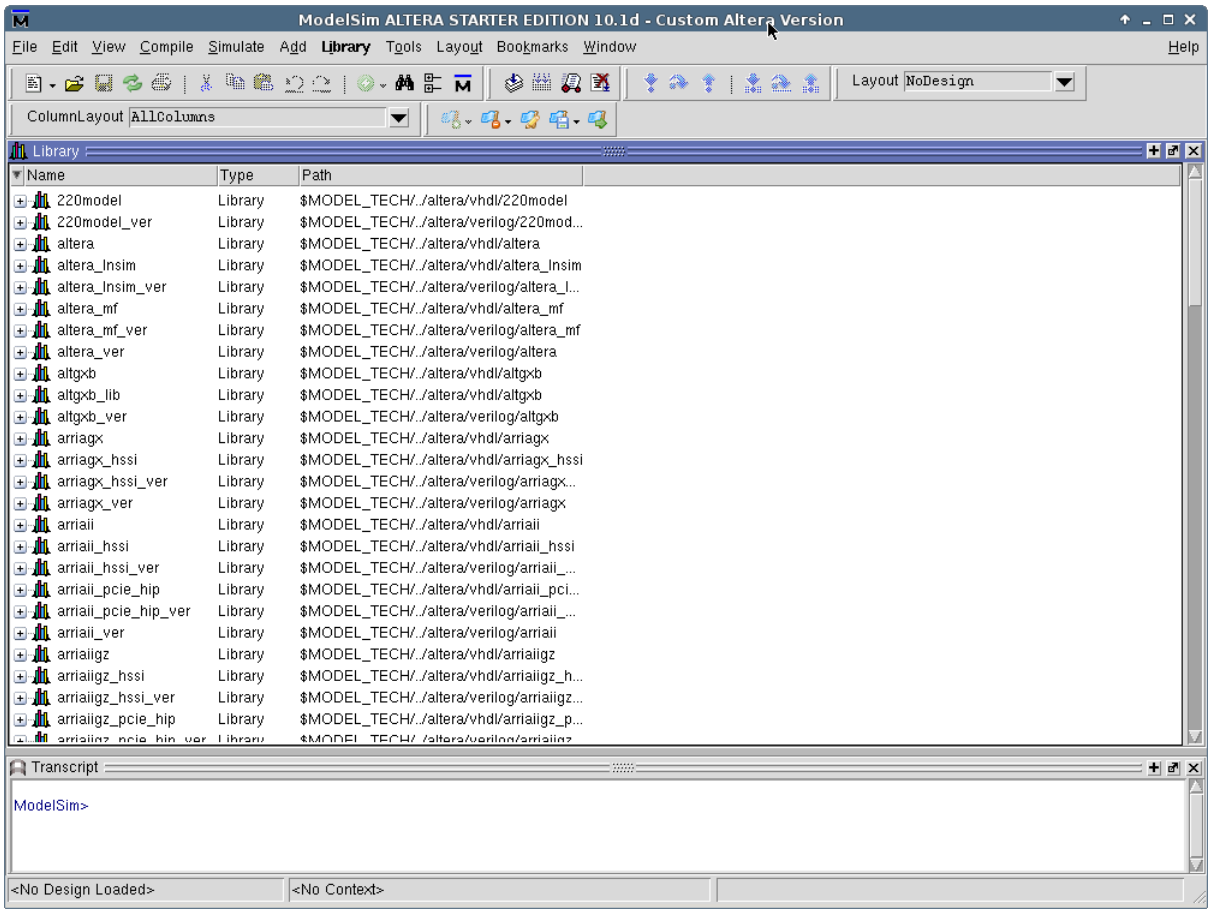
Starting ModelSim

- Click on the ModelSim icon to start
  - A Welcome Screen appears (if run for the first time)
  - To skip this, check on the *'Don't show…'* check-box



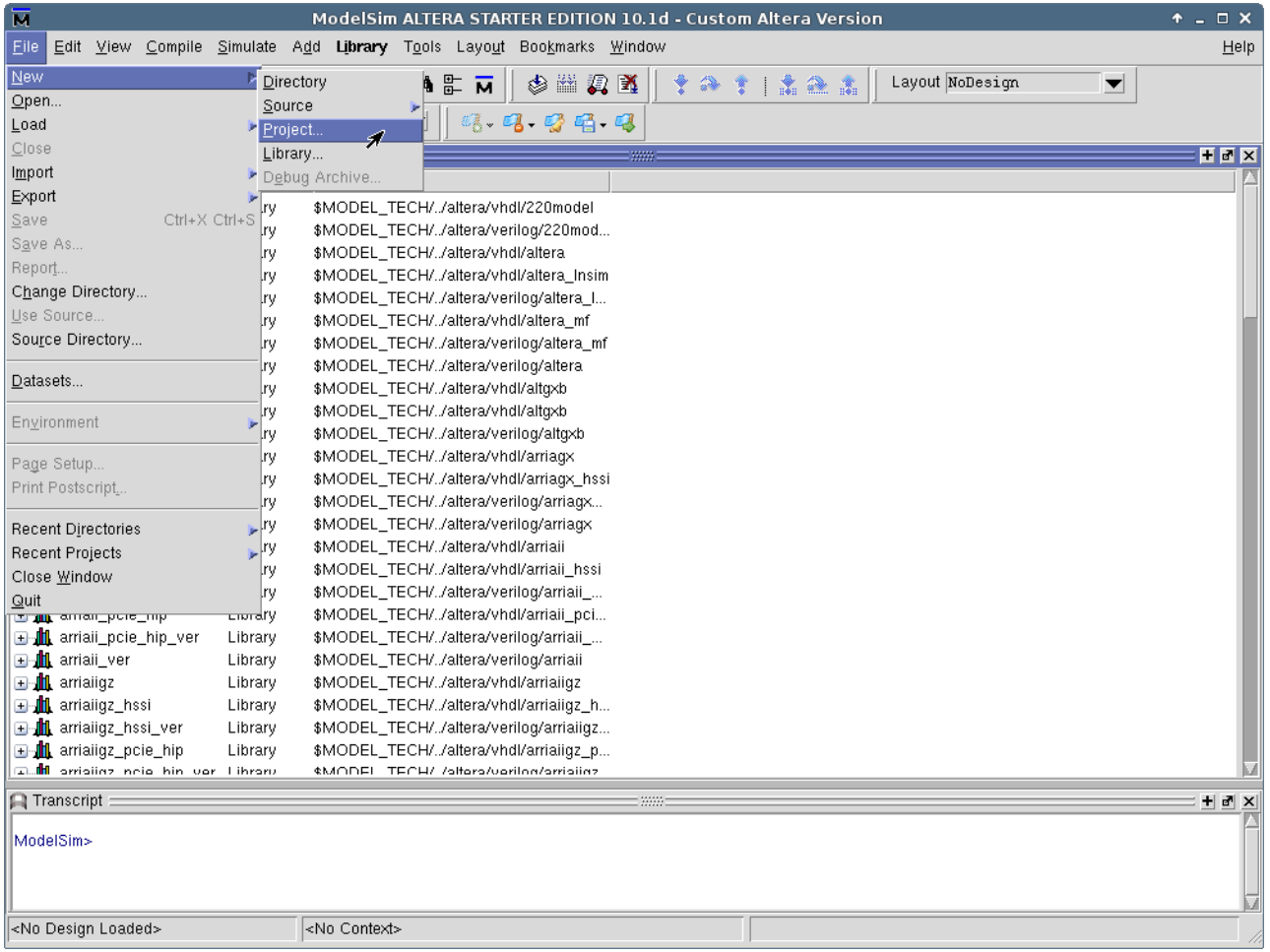
Main Screen

- The main screen shows available libraries
- Let's create a project to work on…



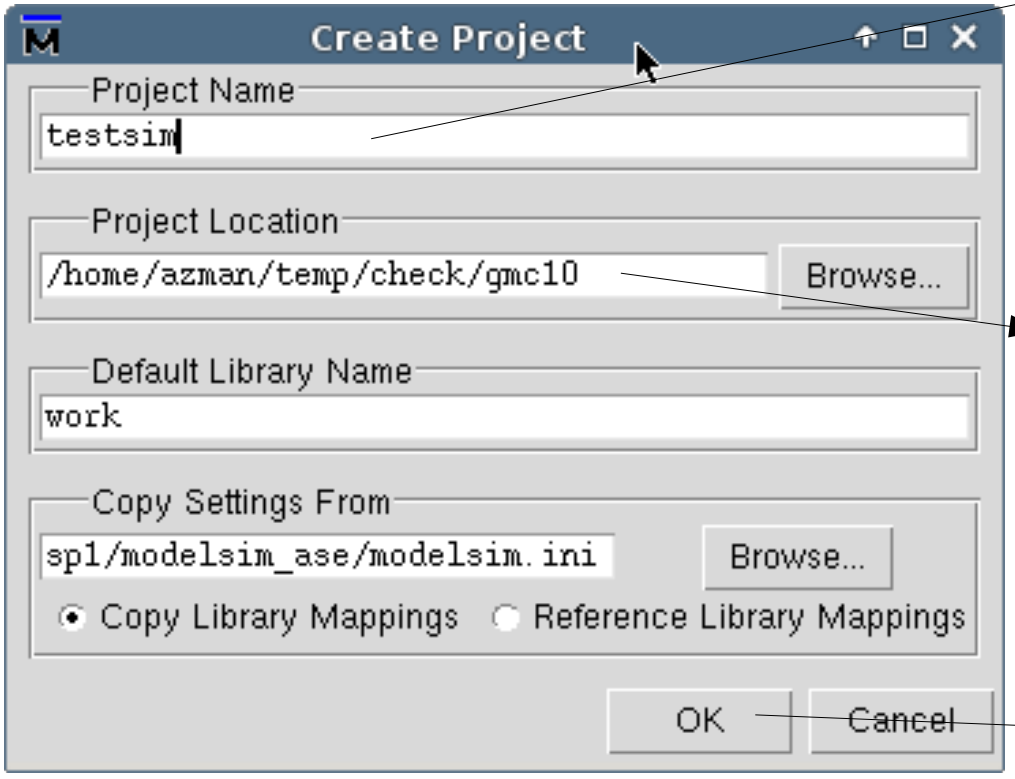
Menu: Create New Project

- Select 'File > New > Project...'



Creating a Project

- Dialog box to create a new project:



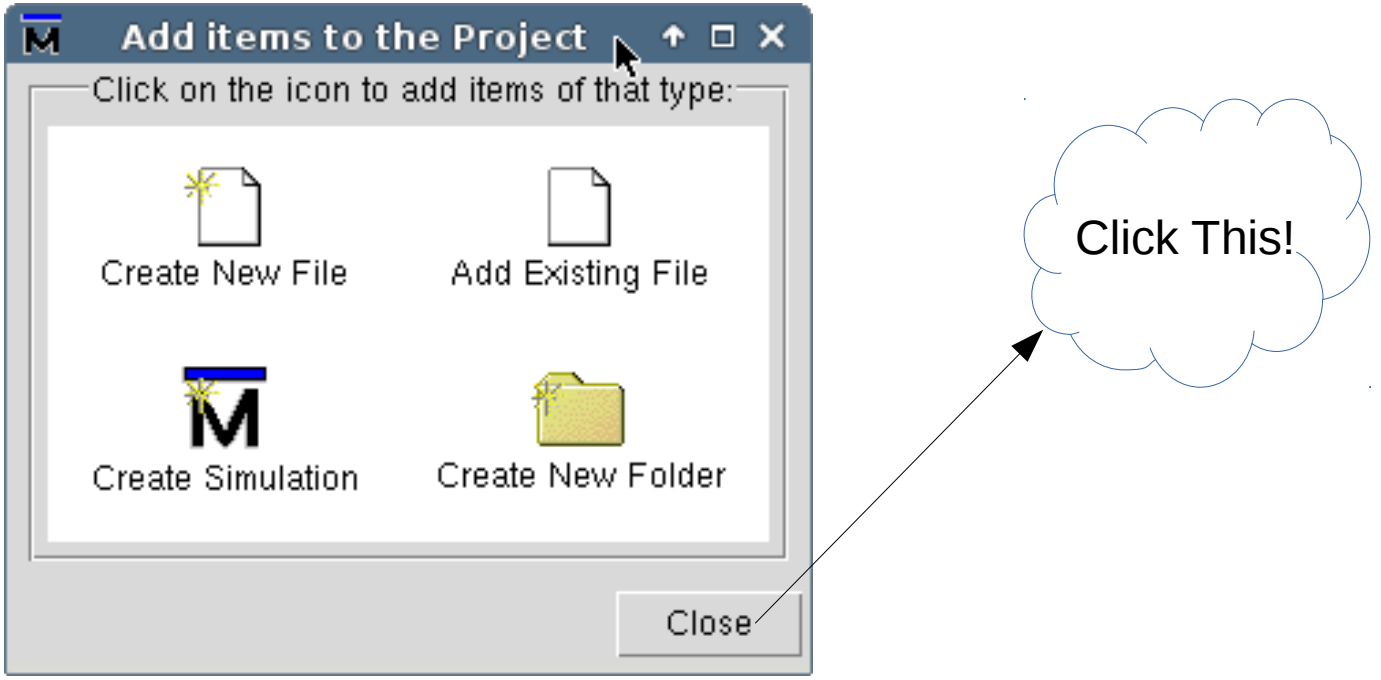
Enter a project Name here

Enter the path: c:\users\public\modelsim\<name>

Click This!

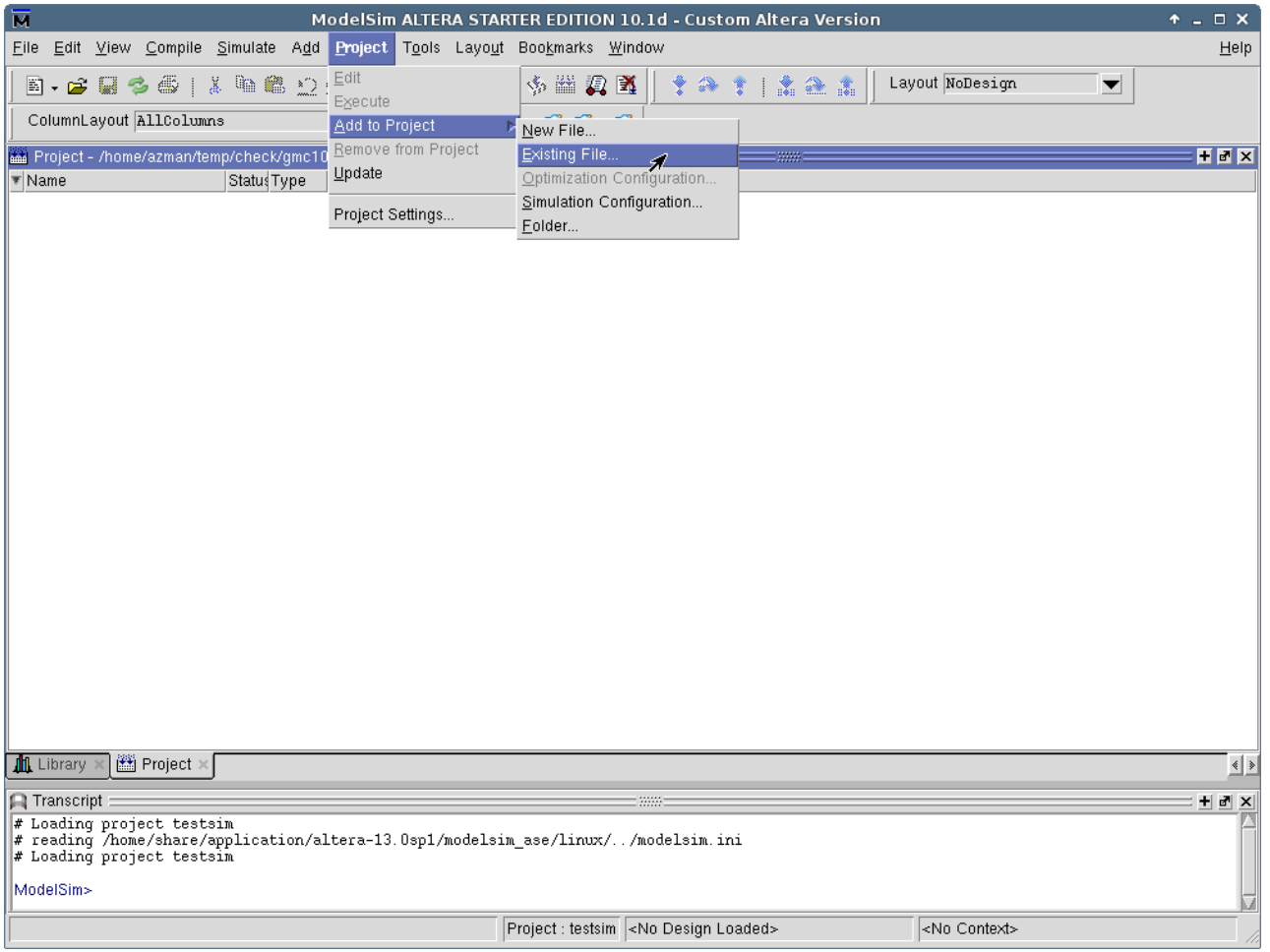
Adding Items

- You will be given a chance to select next task
  - You may use this, or get those options for menu



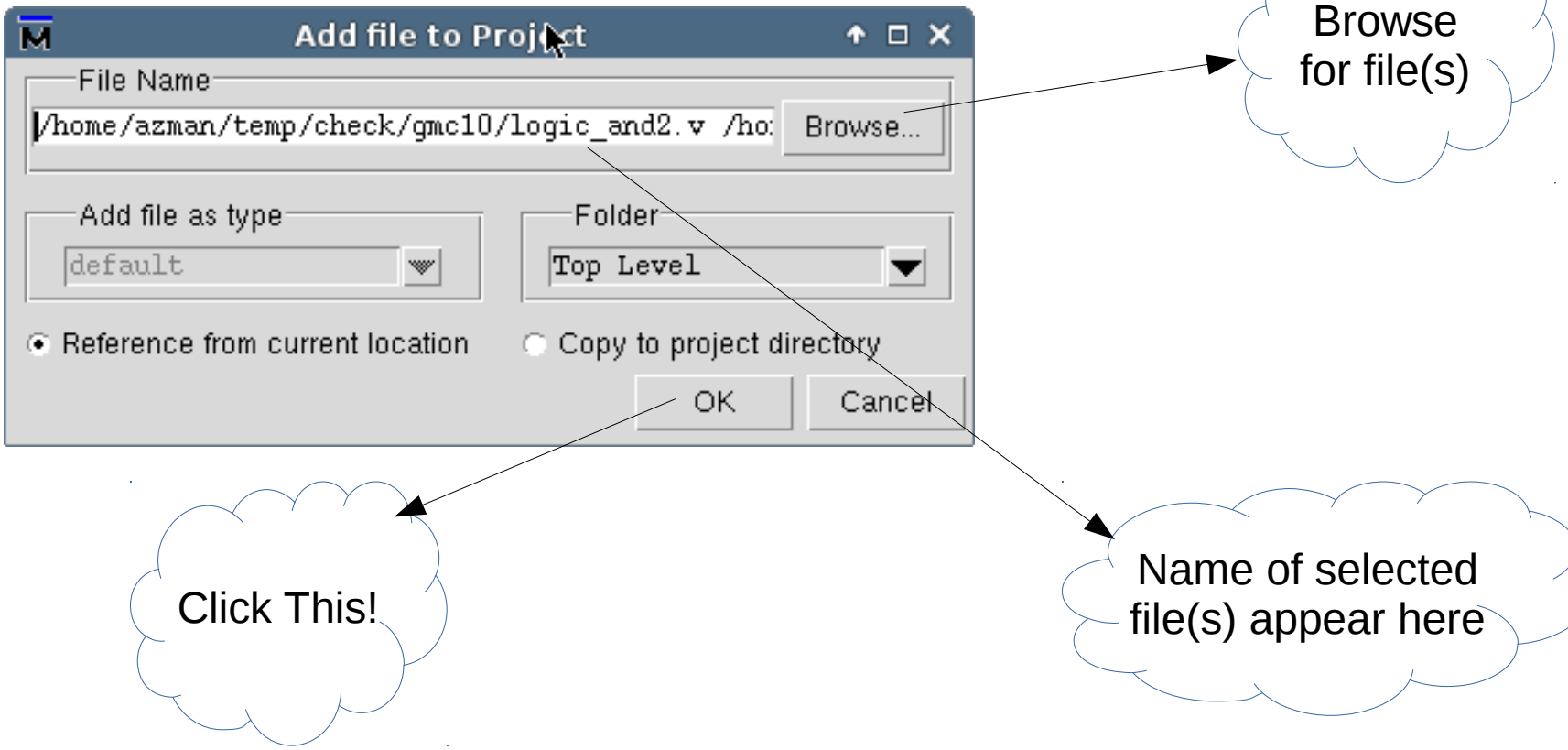
Adding Items (cont.)

- Select *'Project > Add to Project > Existing File…'*



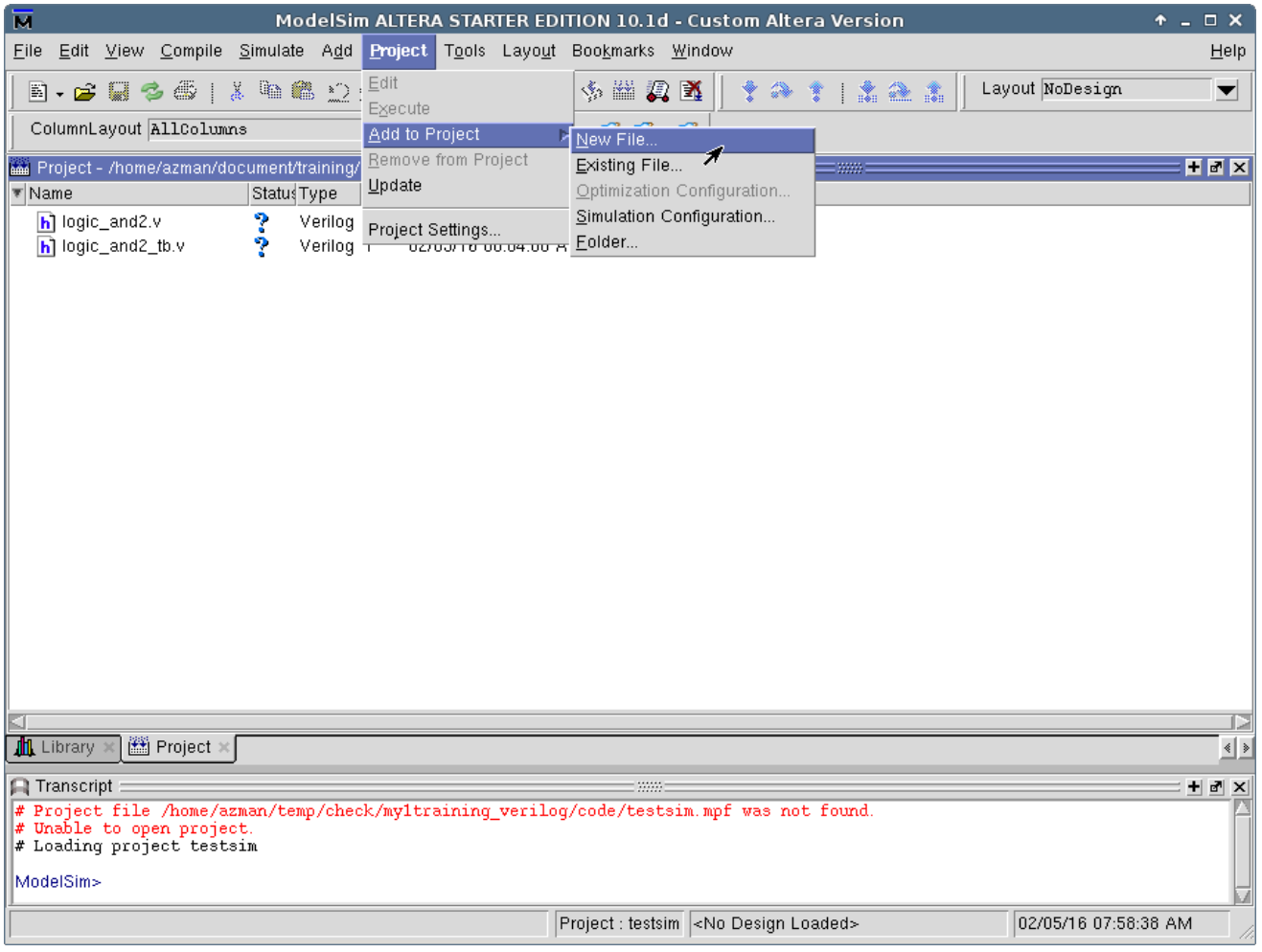
Add Existing Files to Project

- You can browse for your file(s) and add multiple selections to your project
  - select previously created files



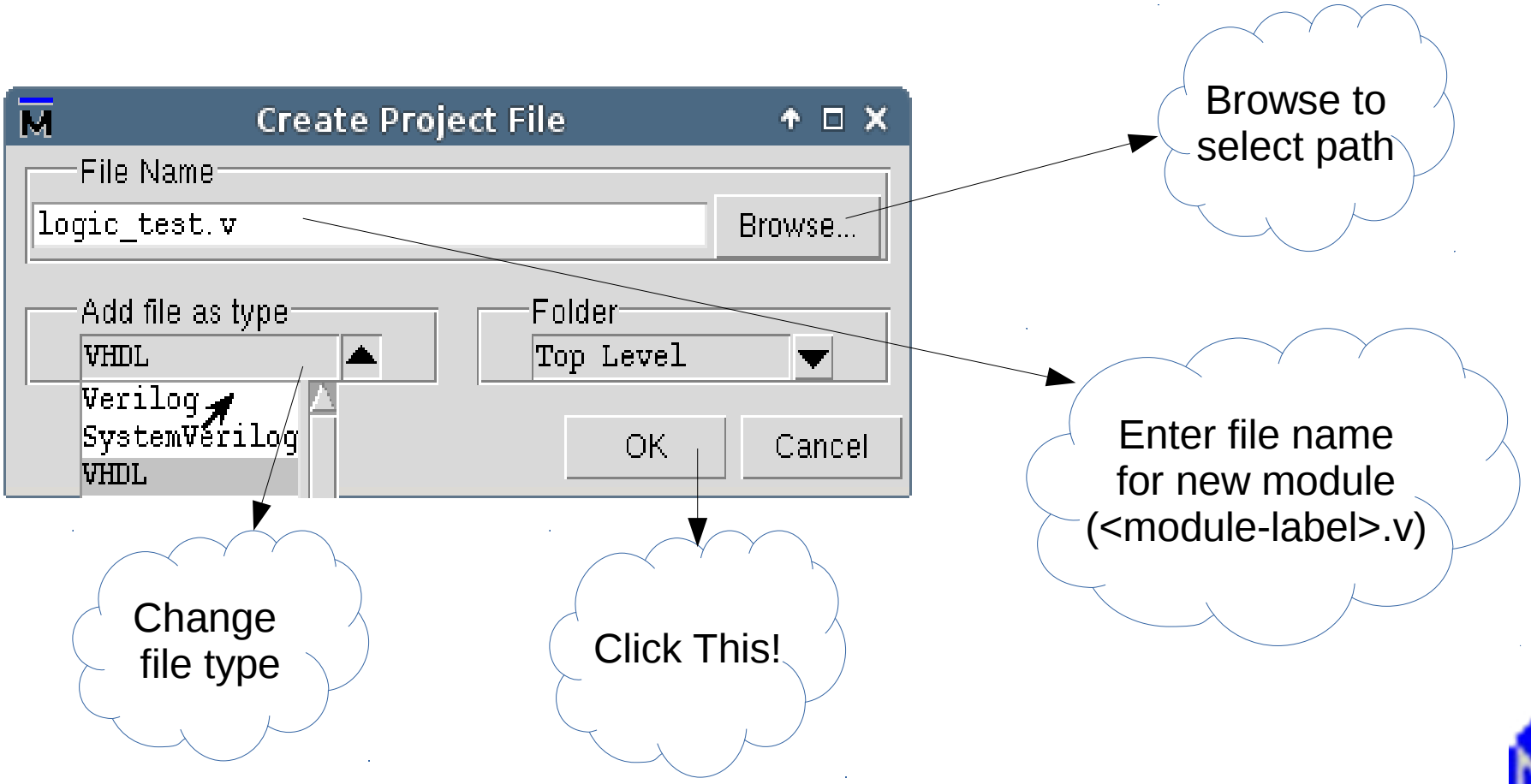
Adding New Items

- Select *'Project > Add to Project > New File…'*



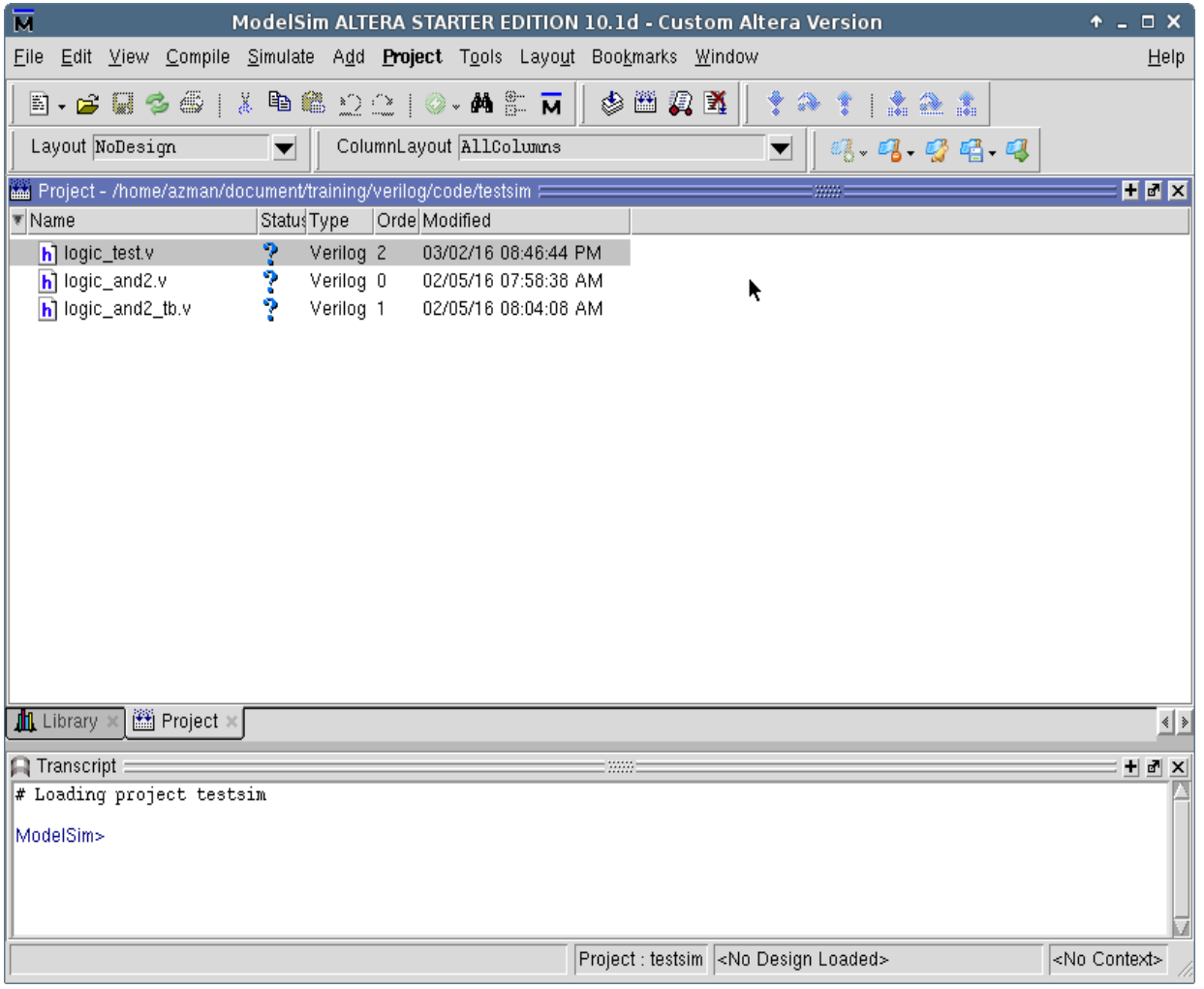
Add New Files to Project

- Provide a suitable filename (*.v)
  - Default path is the project path



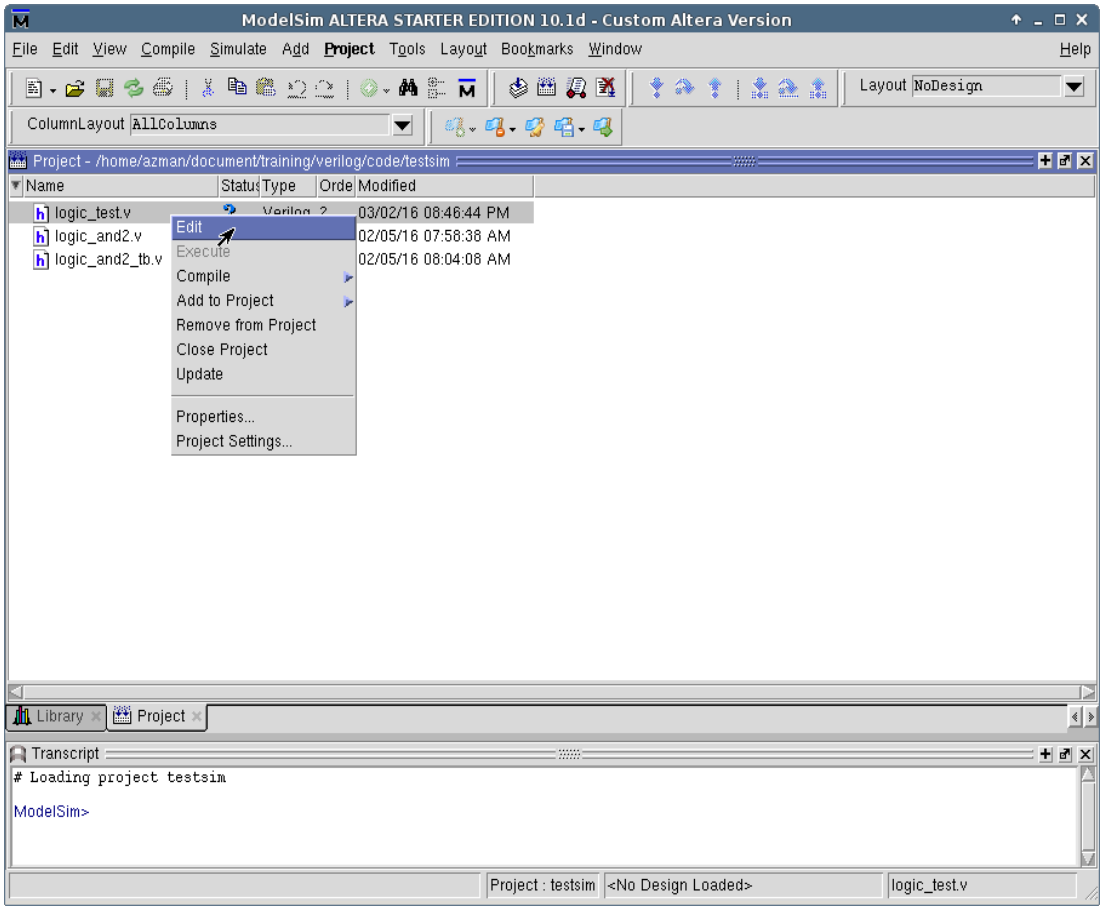
Project View with Loaded Files

- You should see the selected files...



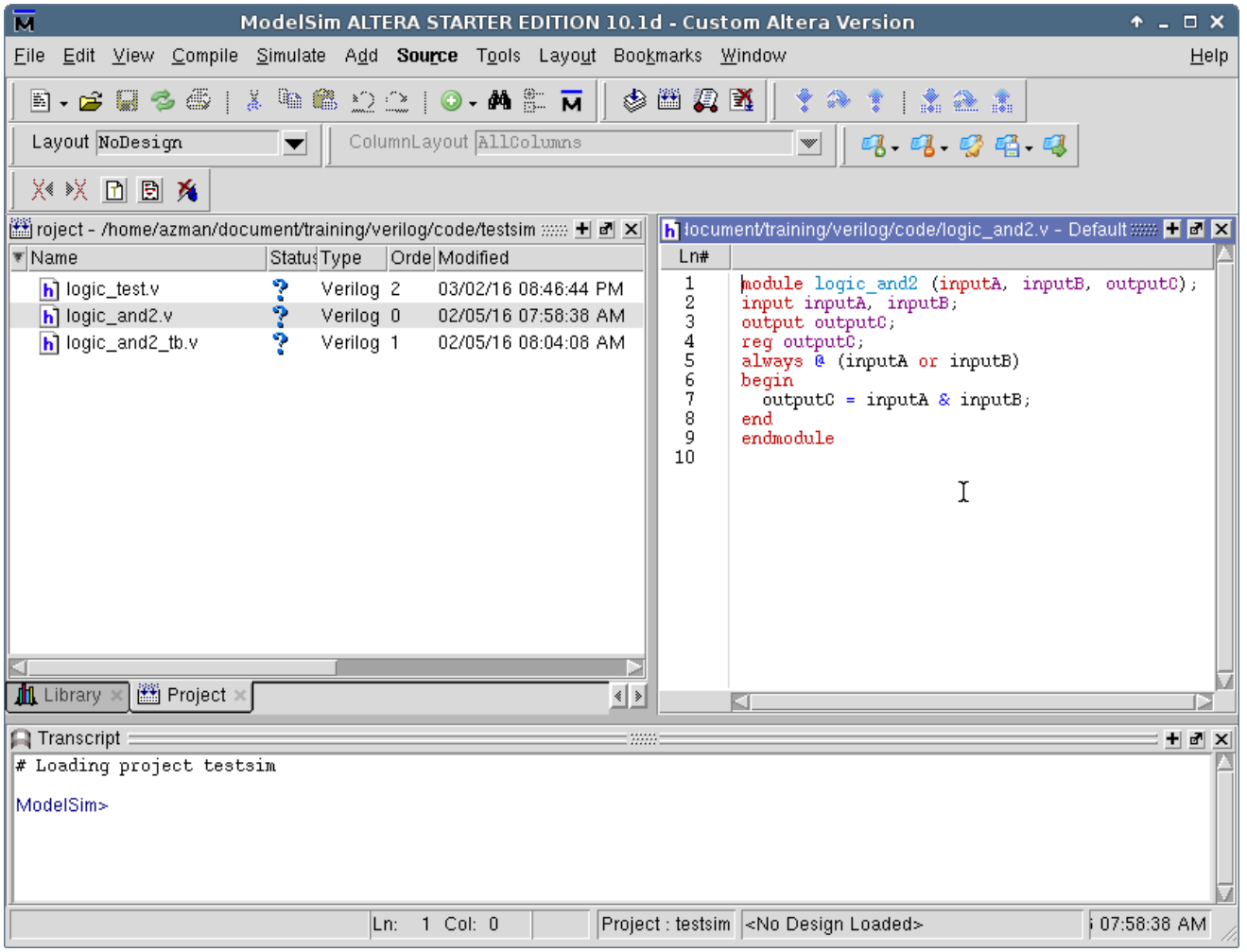
Menu: Edit Verilog Source

- Right click on a source file and select 'Edit'
  - Or, simply double-click on filename



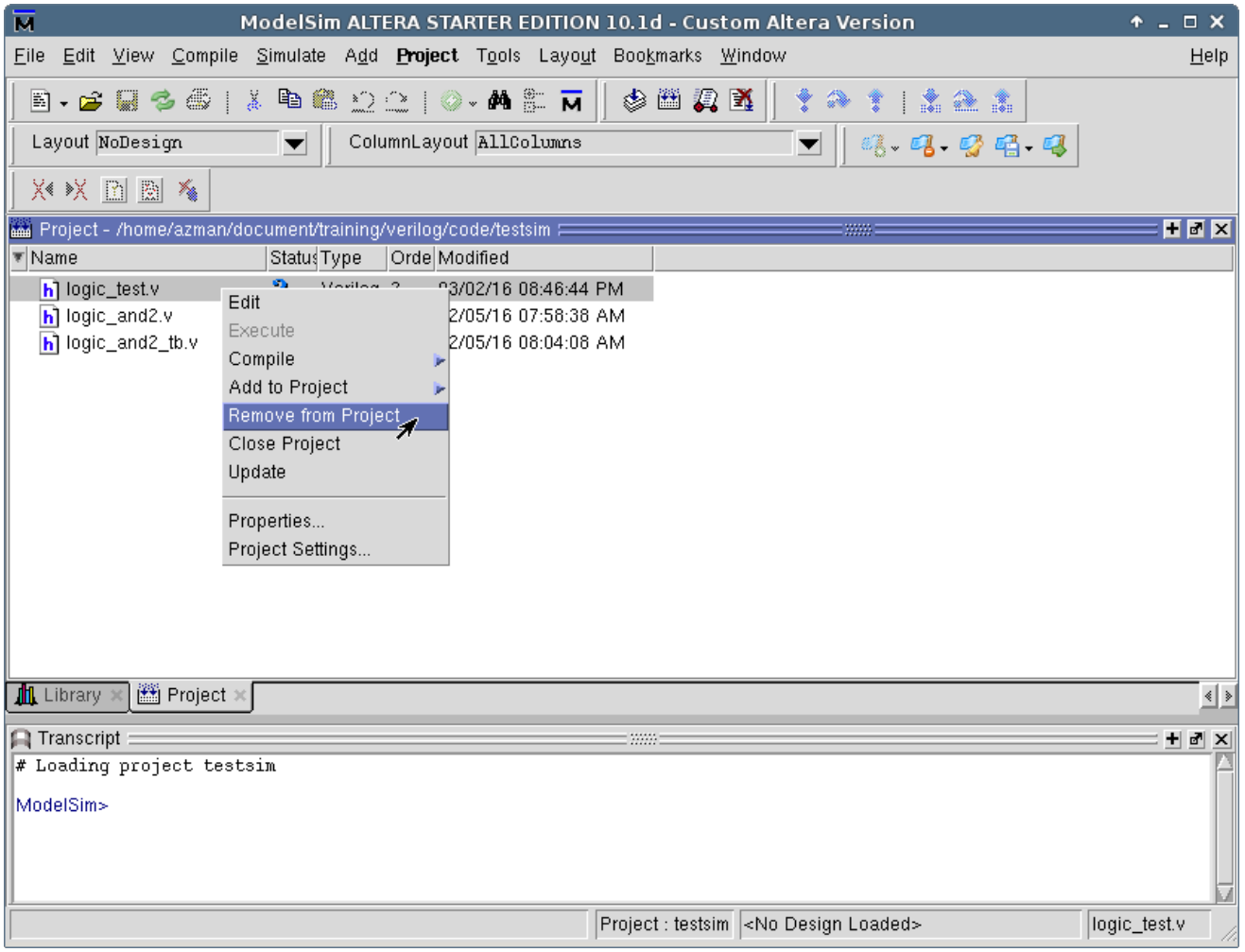
Editing Verilog Source

- You can create/modify source from within



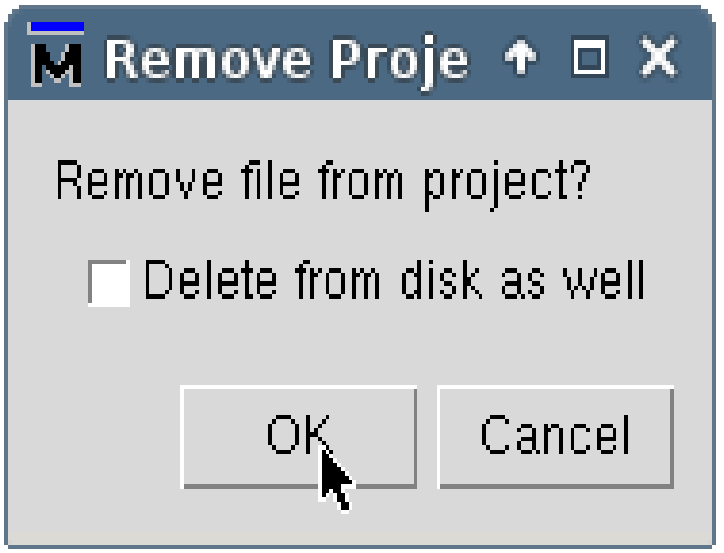
Menu: Remove Verilog Source

- You can remove source from a project



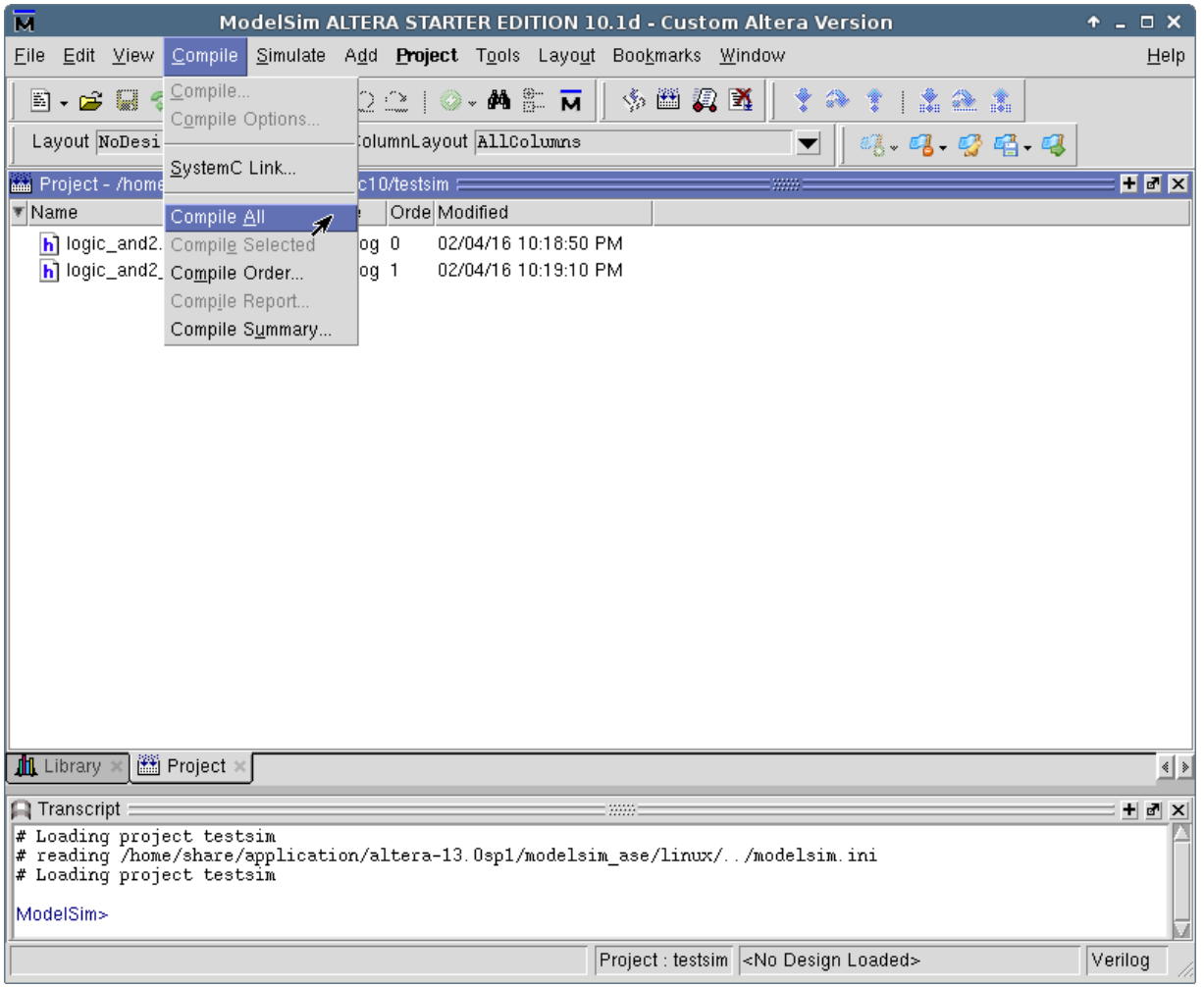
Removing Verilog Source

- With option to delete



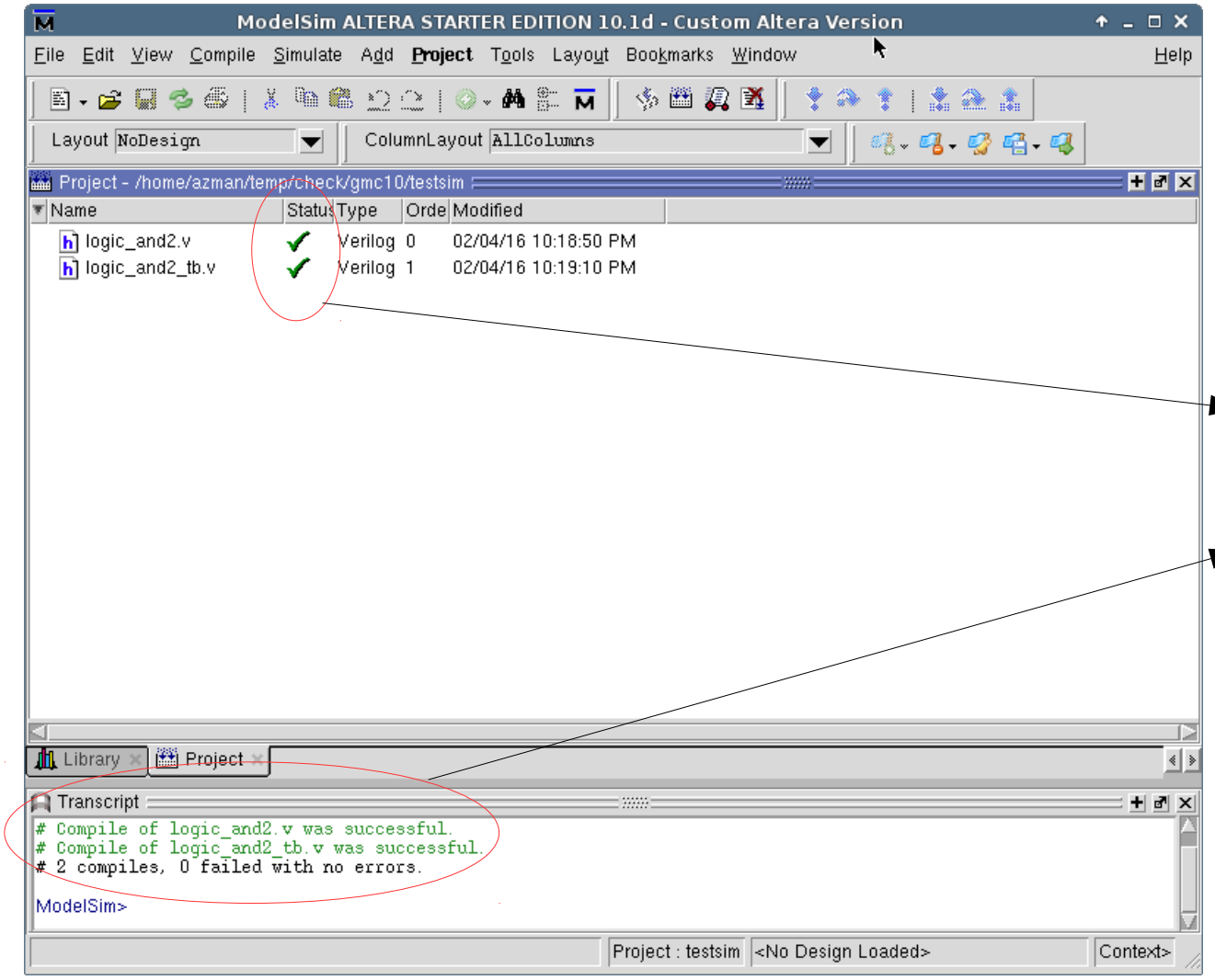
Menu: Compile Verilog Source

- To compile, select 'Compile > Compile All'



Compile Verilog Source

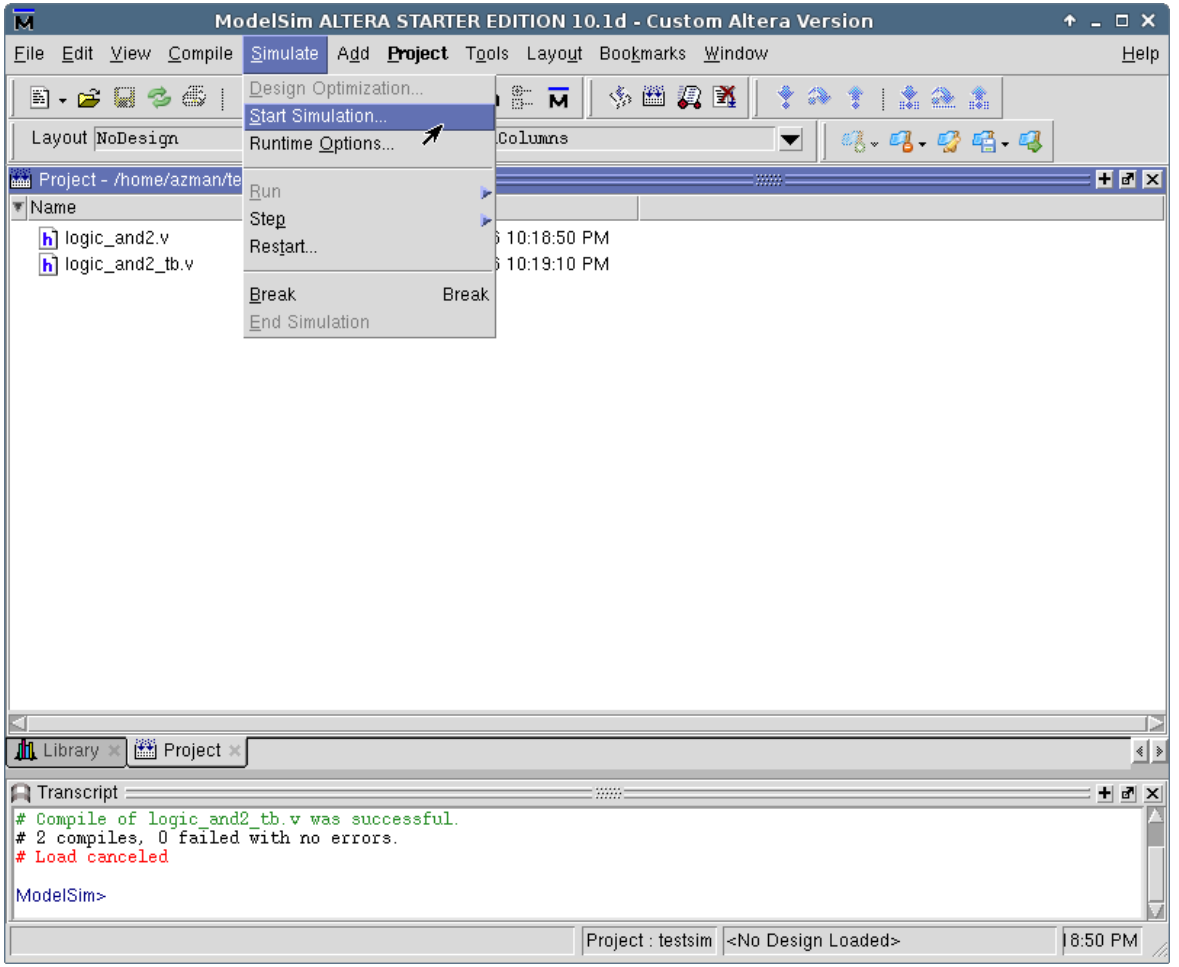
- Once completed you should see notifications



Positive results!
Syntax is okay.
It DOES NOT mean that your design is correct!

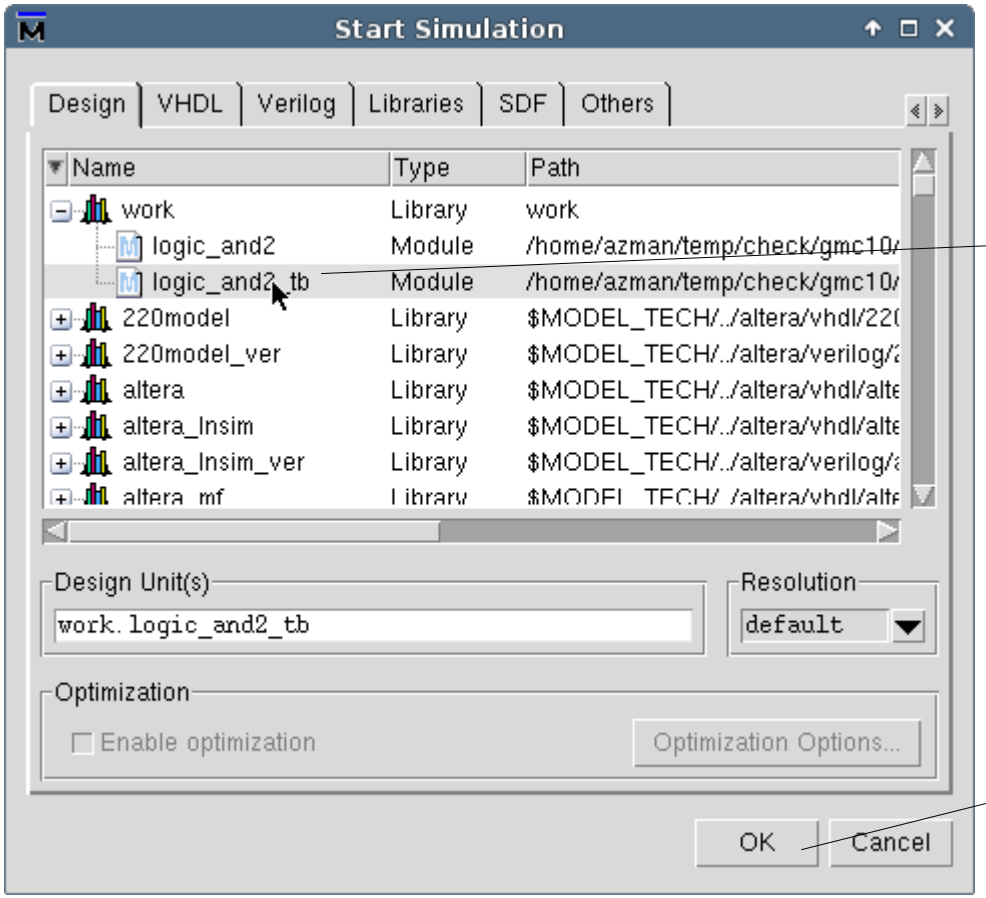
Menu: Simulate

- Select 'Simulate > Start Simulation…'



Simulating Design

- Select your testbench code

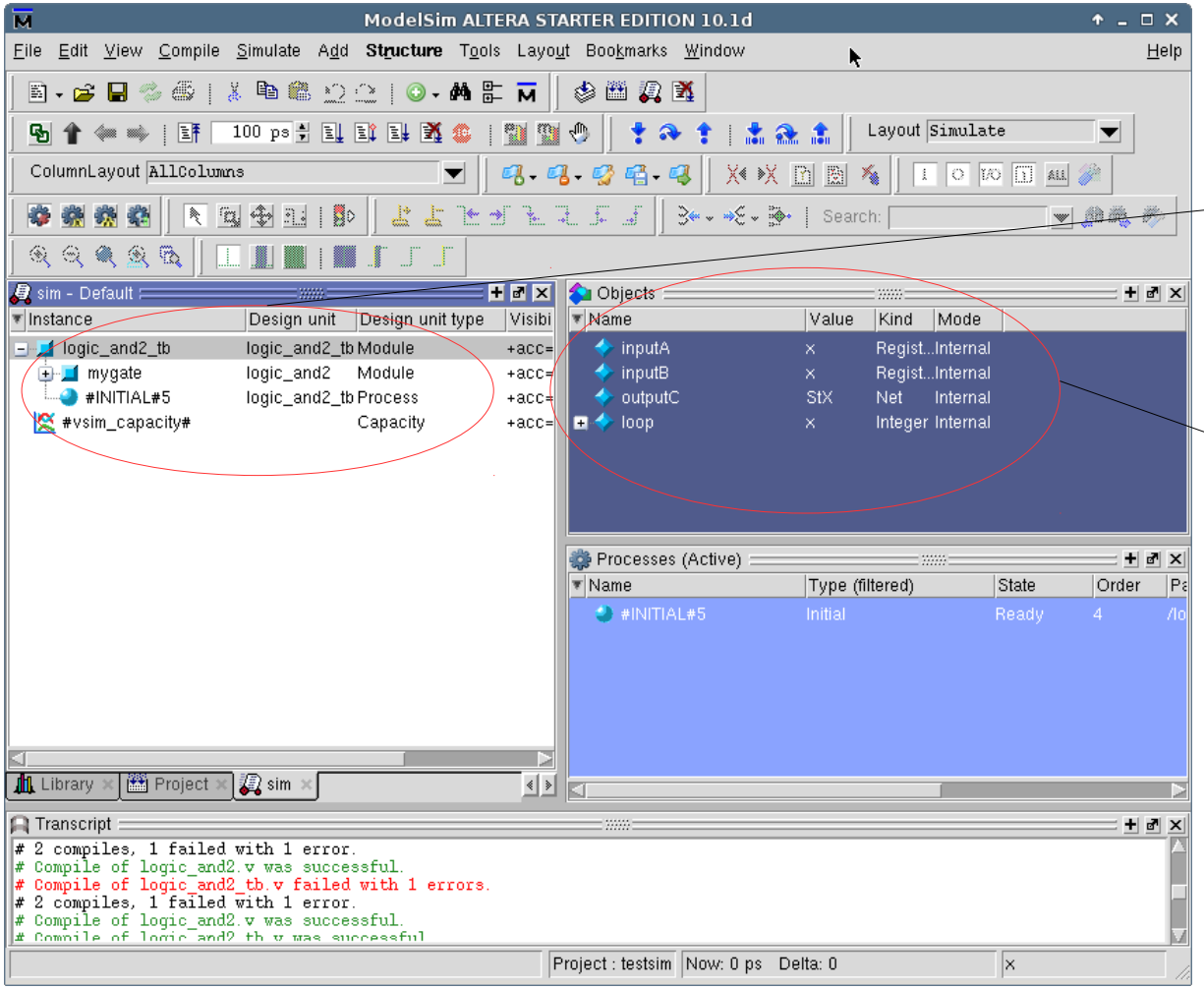


Select your testbench module from 'work'

Click This!

Simulating Design (cont.)

- Once loaded you should see your module(s):

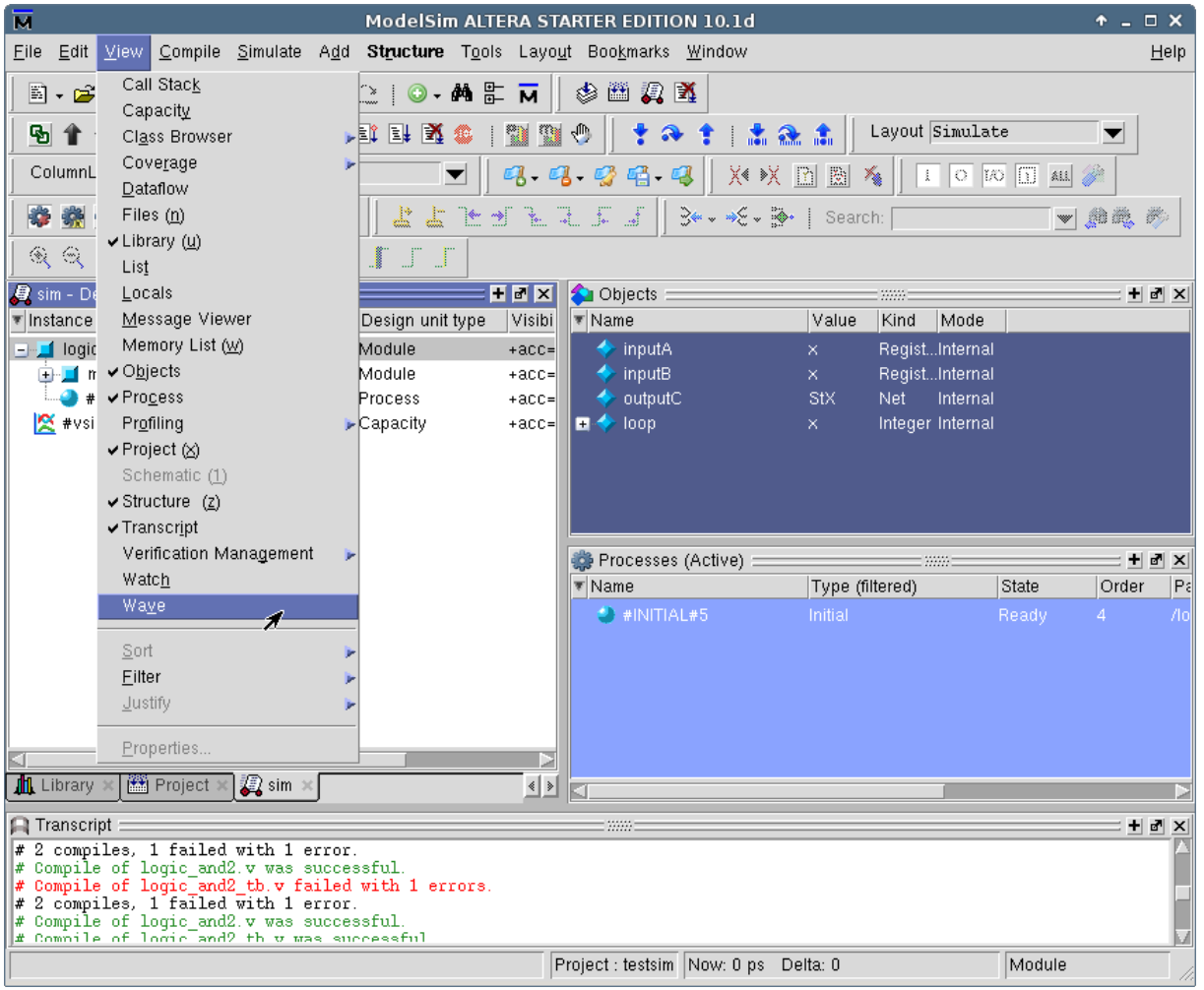


Loaded modules

Signals that can be analyzed

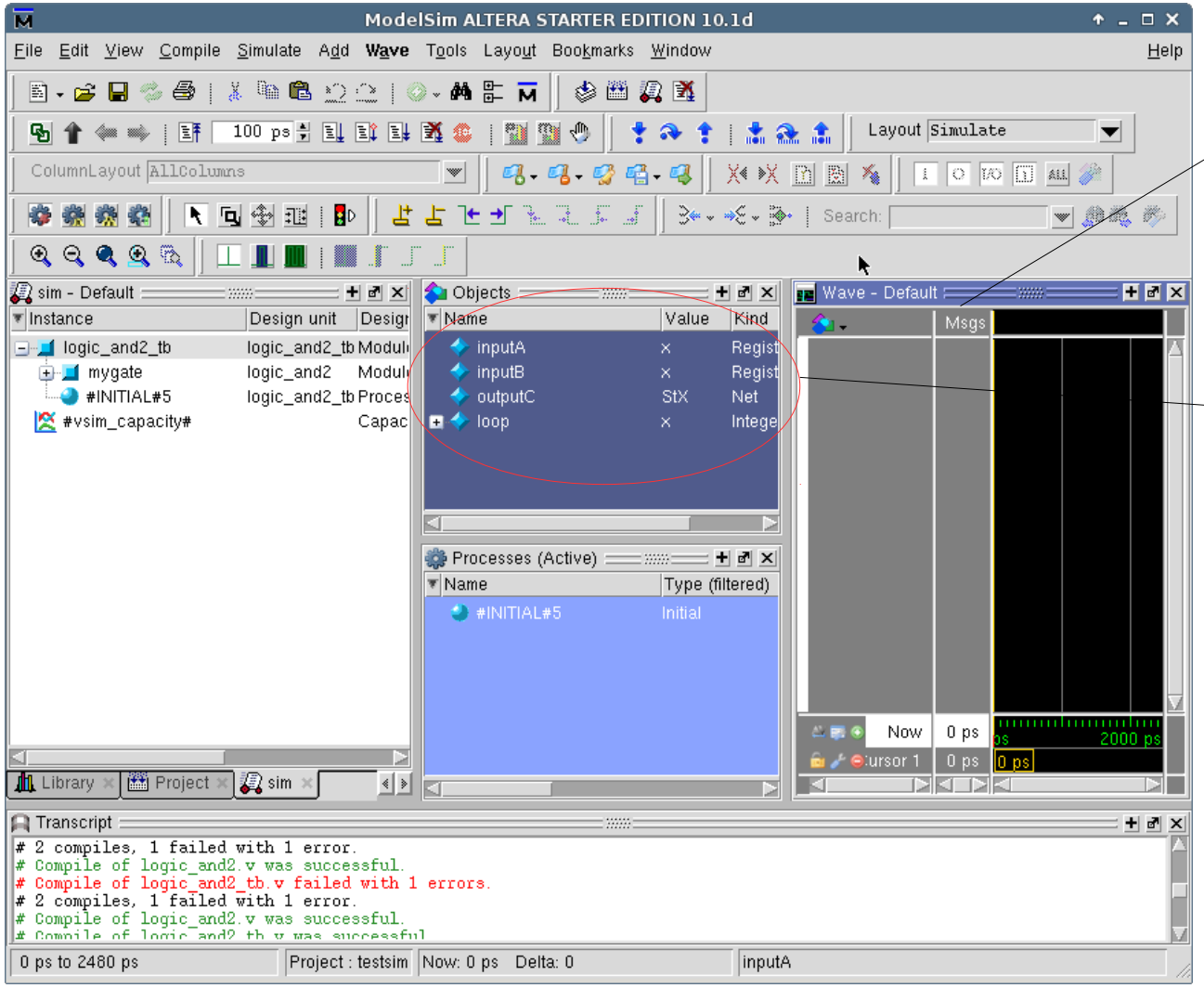
Menu: Waveform Viewer

- Select 'View > Wave'



Waveform Viewer

- Appears as sub-window (on first run)

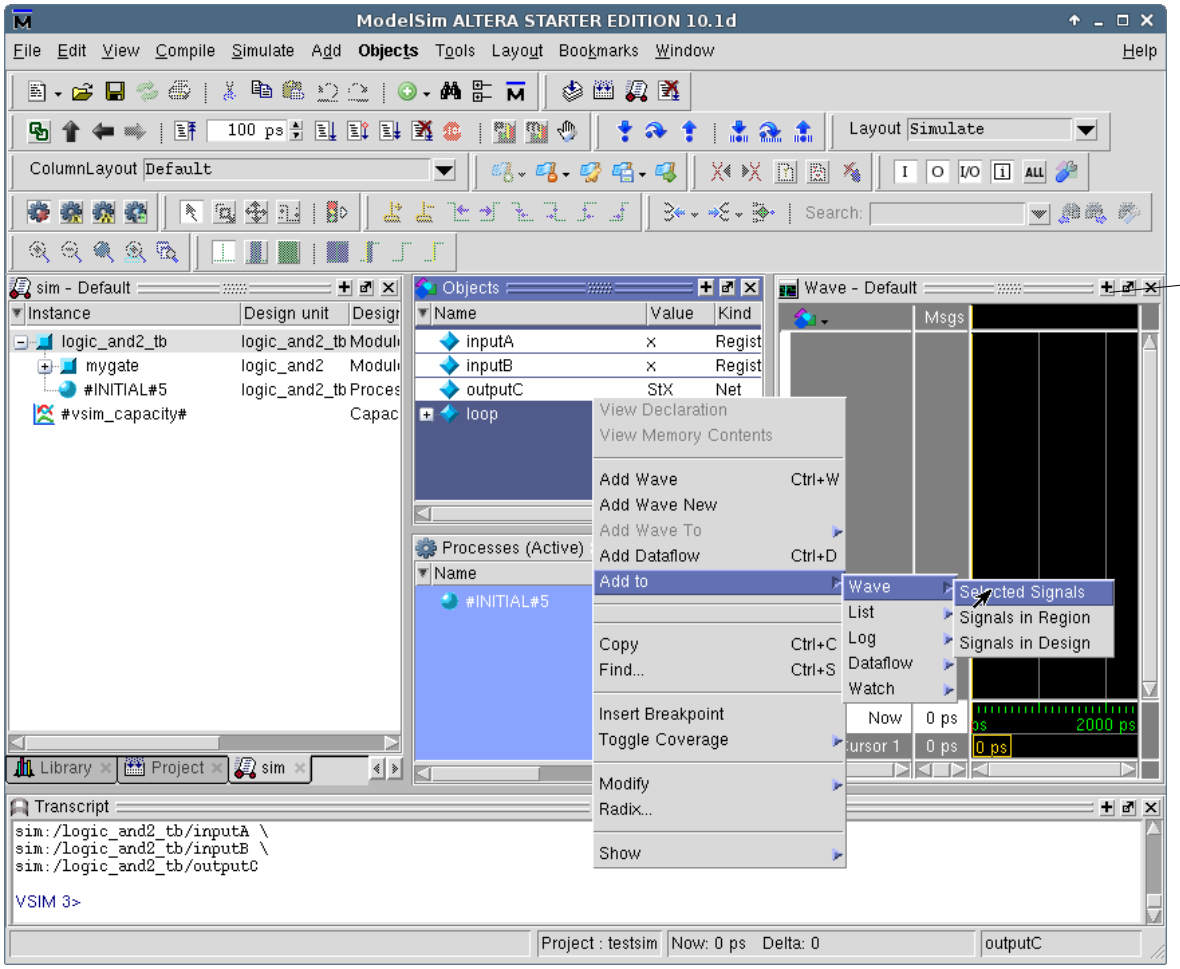


Wave viewer window

Select signal(s) to view

Wave Viewer: Adding Signals

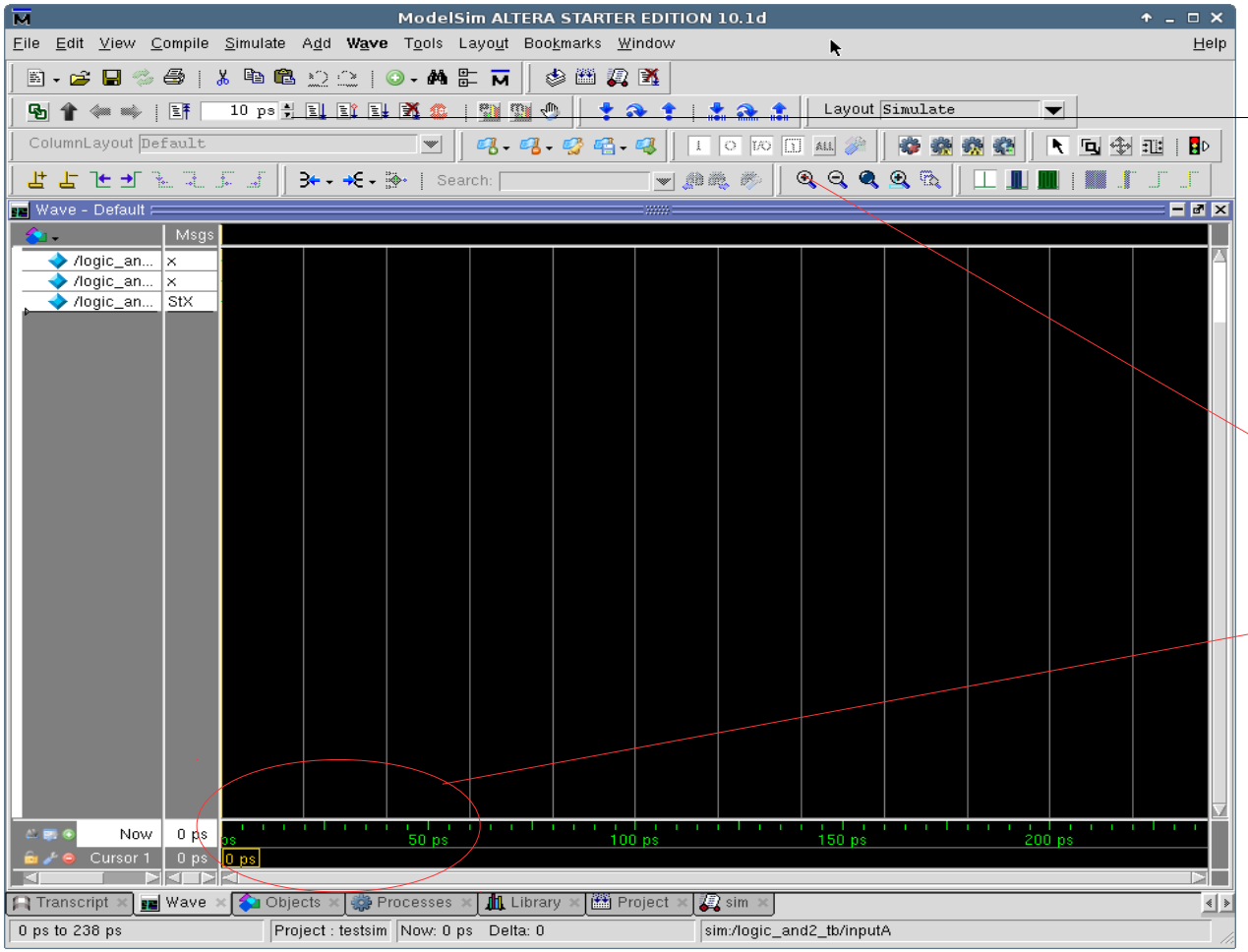
- Select signals (Ctrl-click) inputA,inputB,outputC
  - Right-click, select 'Add to >Wave >Selected signals'



Click this when done to enlarge window

Ready to Execute (Simulation)

- Change a few settings...

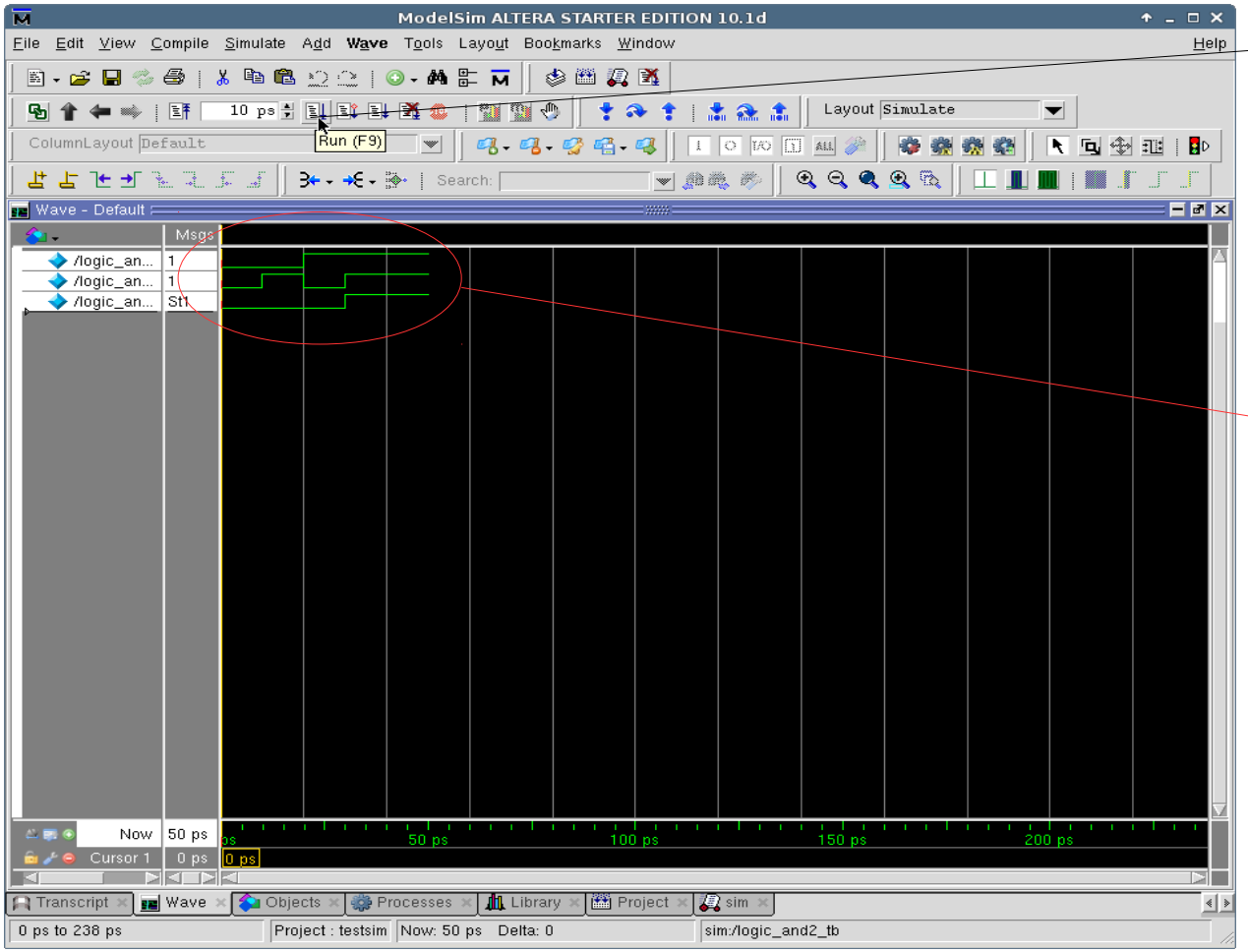


Set run-step to 10 ps

Zoom scale to 5 ps

Executing/Running the Simulation

- Click on Run (F9) icon...

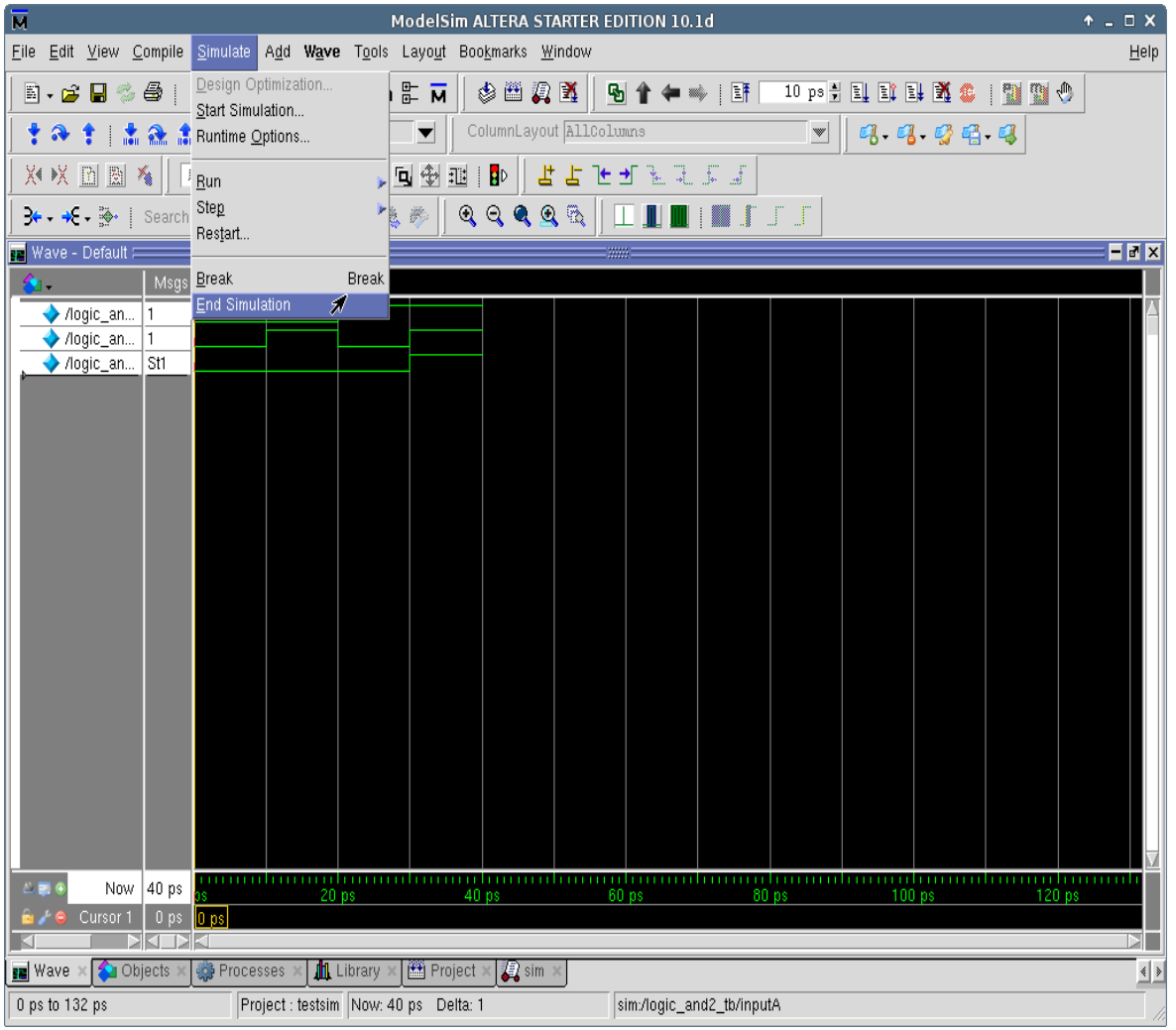


Each click runs 10 ps

Analyze This!

Running New Simulation

- To run a new simulation, end the current simulation



Practical Session 3.1

- Implement the given logic in truth table
  - You may choose to use 'assign' statements or 'always' block
- Create a suitable testbench for the modules
- Simulate and analyze the results to verify the functionality of the modules

iA	iB	iC	oD
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0