Introduction to Verilog and ModelSim

(Part 3 – Using ModelSim)



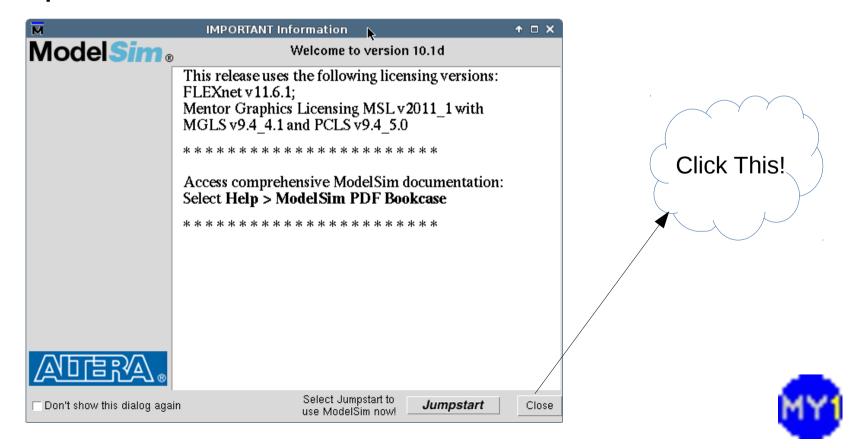
HDL Simulator

- ModelSim
 - Widely used in the industry
 - Can simulate either/both VHDL or/and Verilog
 - Has GUI interface (editor, waveform viewer)
- Alternative: Icarus Verilog
 - Open source simulation tool
 - Purely a Verilog simulator
 - Requires separate waveform viewer



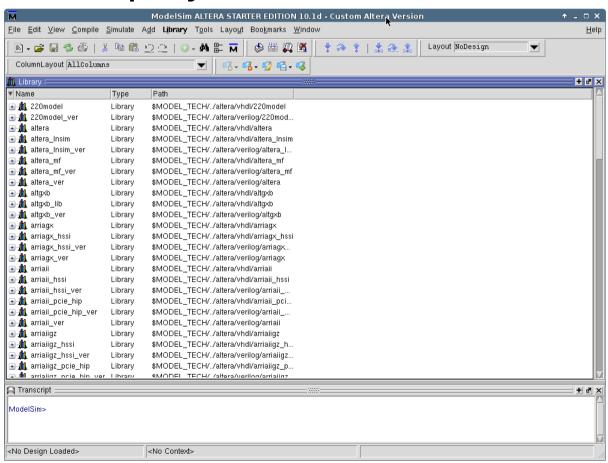
Starting ModelSim

- Click on the ModelSim icon to start
 - A Welcome Screen appears (if run for the first time)
 - To skip this, check on the 'Don't show...' check-box



Main Screen

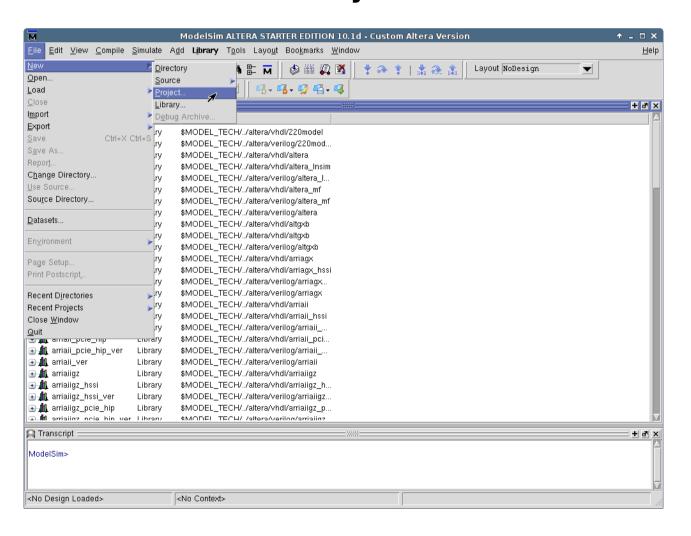
- The main screen shows available libraries
- Let's create a project to work on...





Menu: Create New Project

Select 'File > New > Project...'



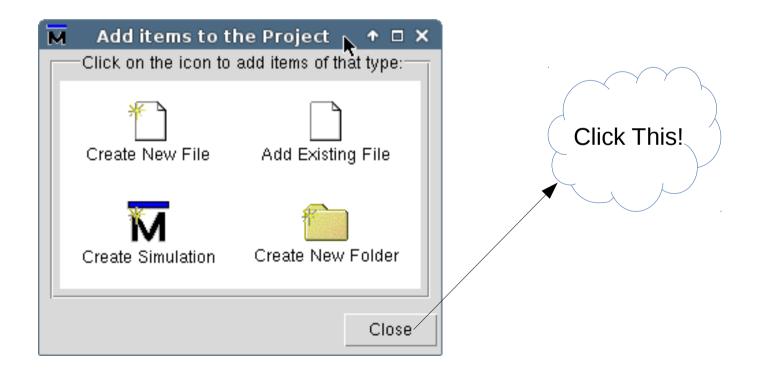


Creating a Project

 Dialog box to create a new project: Enter a project Name here м Create Project ↑ 🗆 X Project Name testsim Project Location /home/azman/temp/check/qmc10 Browse... Enter the path: Default Library Name c:\users\public\modelsim\<name> work. Copy Settings From sp1/modelsim ase/modelsim.ini Browse... Copy Library Mappings
 Reference Library Mappings OK. Cancel Click This!

Adding Items

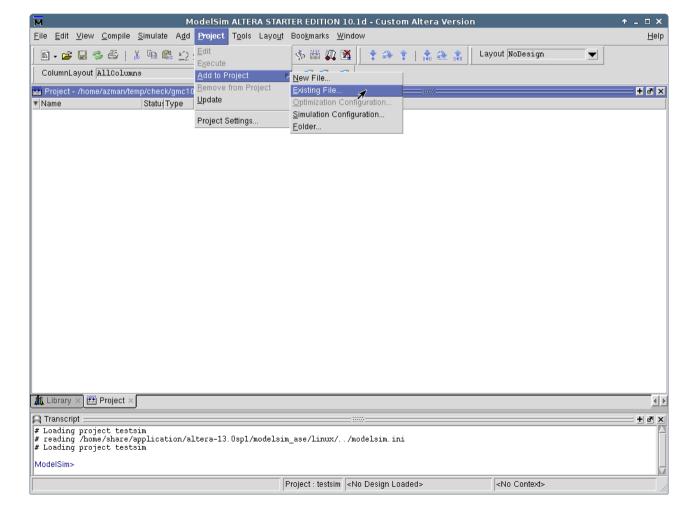
- You will be given a chance to select next task
 - You may use this, or get those options for menu





Adding Items (cont.)

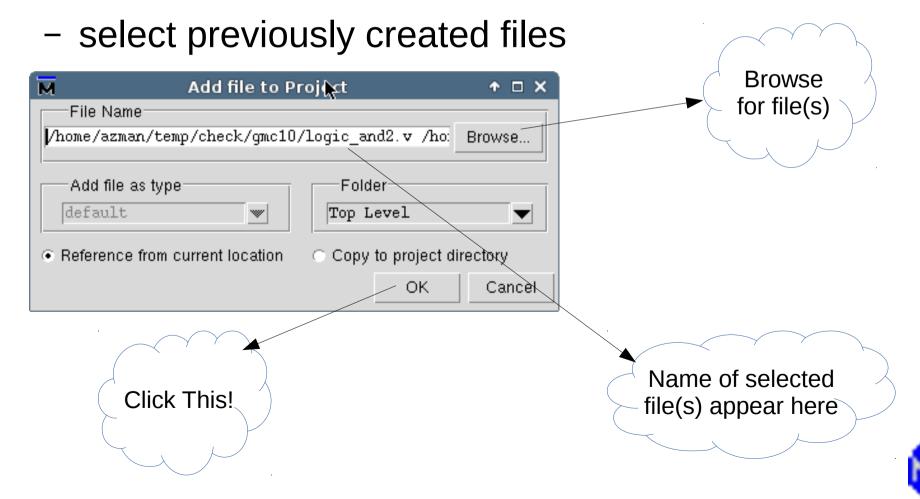
Select 'Project > Add to Project > Existing
 File...'





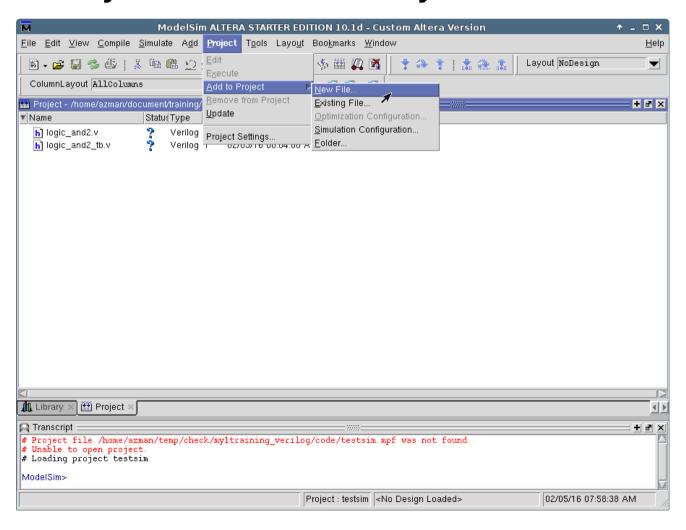
Add Existing Files to Project

 You can browse for your file(s) and add multiple selections to your project



Adding New Items

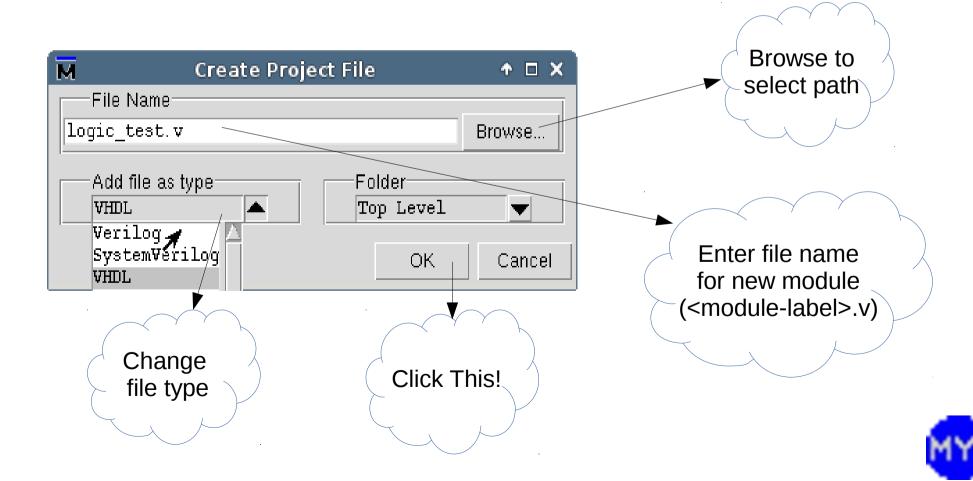
Select 'Project > Add to Project > New File...'





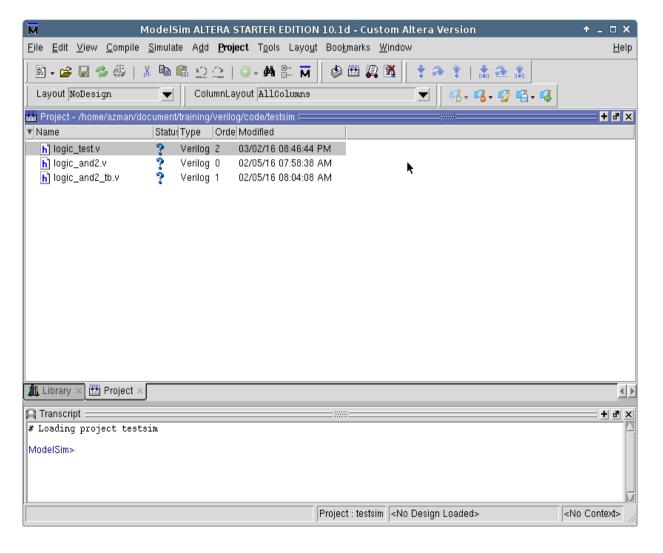
Add New Files to Project

- Provide a suitable filename (*.v)
 - Default path is the project path



Project View with Loaded Files

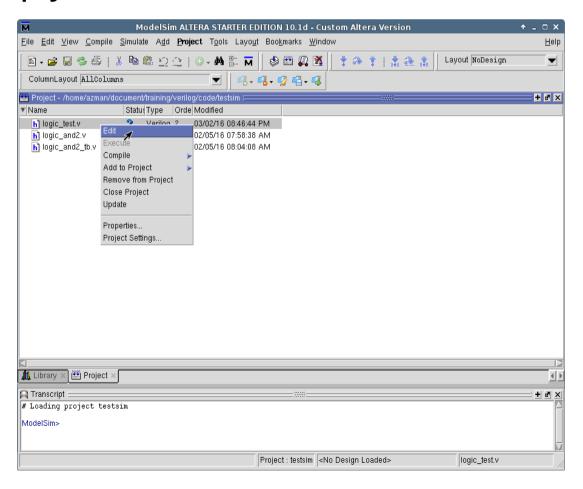
You should see the selected files...





Menu: Edit Verilog Source

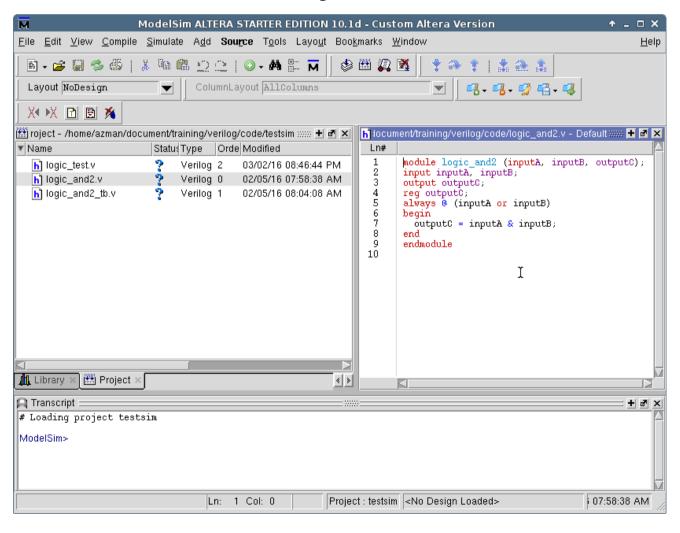
- Right click on a source file and select 'Edit'
 - Or, simply double-click on filename





Editing Verilog Source

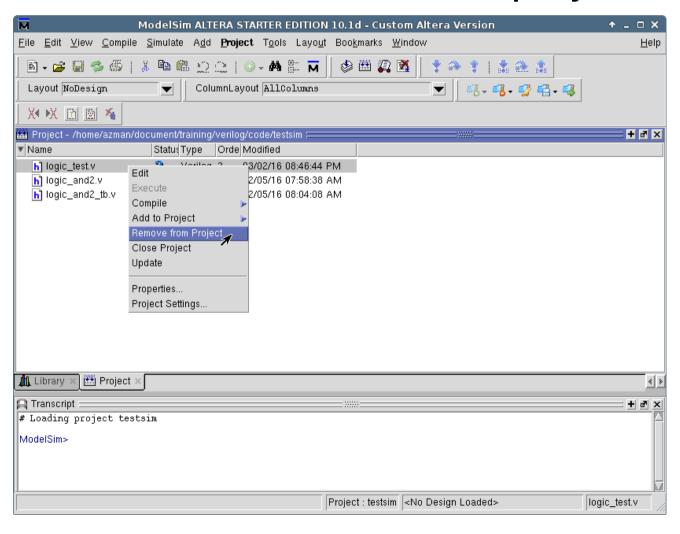
You can create/modify source from within





Menu: Remove Verilog Source

You can remove source from a project





Removing Verilog Source

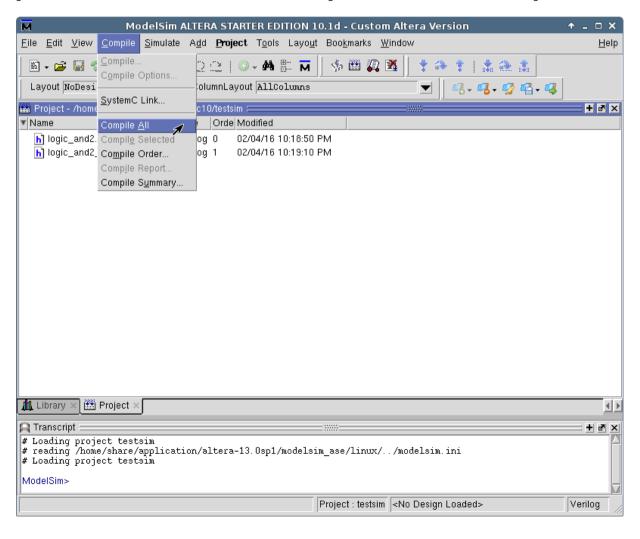
With option to delete

M Remove P	roje ↑ 🗆 🗙 े		
Remove file from project?			
Delete from disk as well			
ΟĶ	Cancel		



Menu: Compile Verilog Source

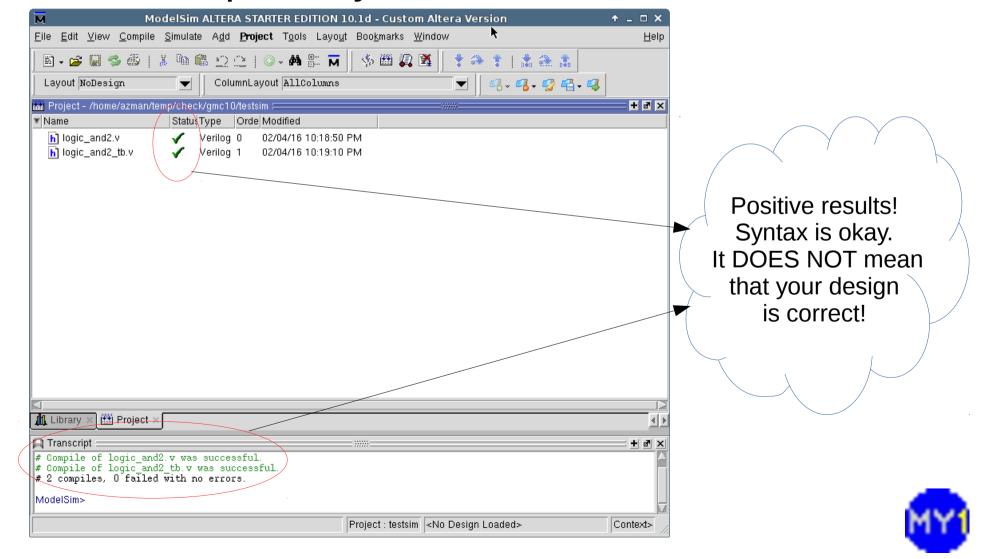
To compile, select 'Compile > Compile All'





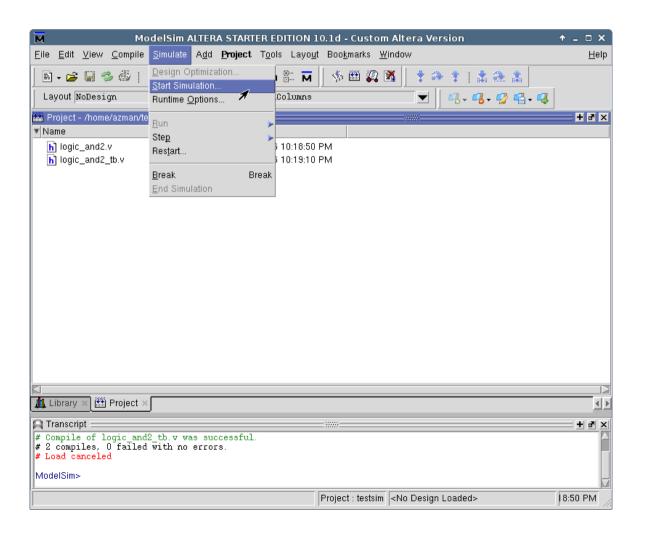
Compile Verilog Source

Once completed you should see notifications



Menu: Simulate

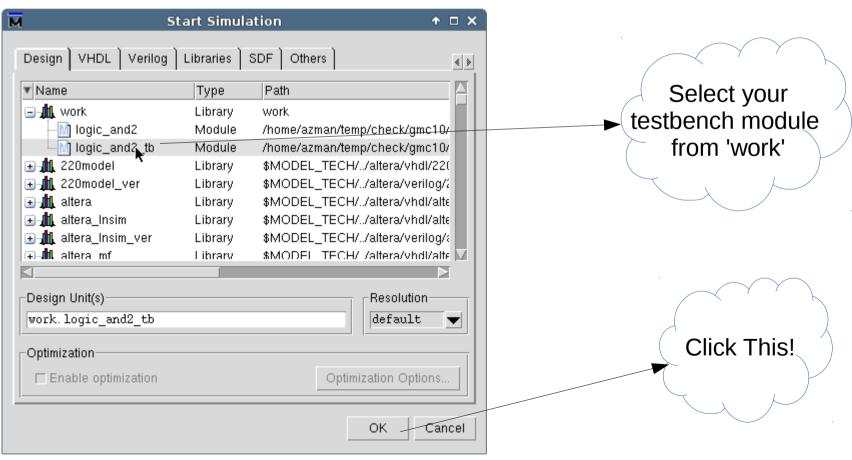
Select 'Simulate > Start Simulation...'





Simulating Design

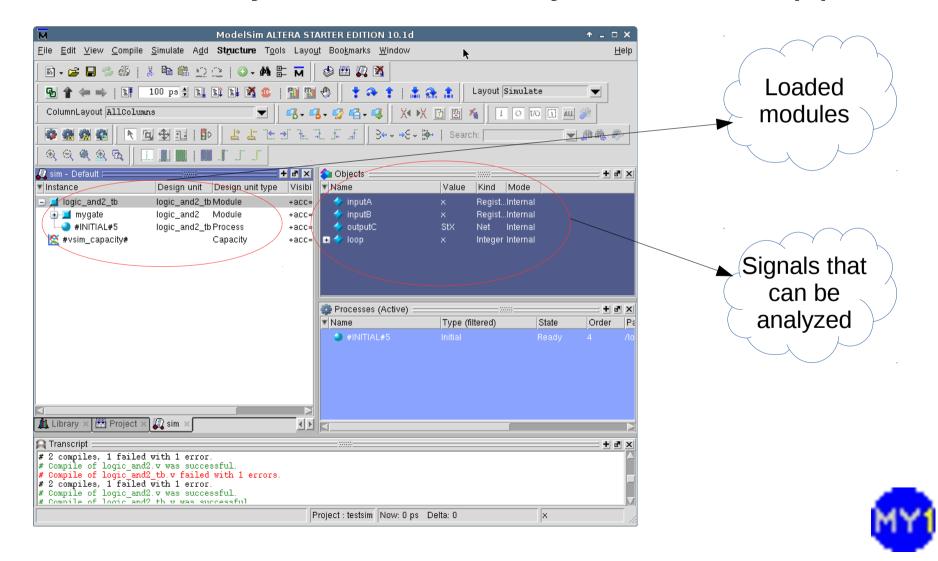
Select your testbench code





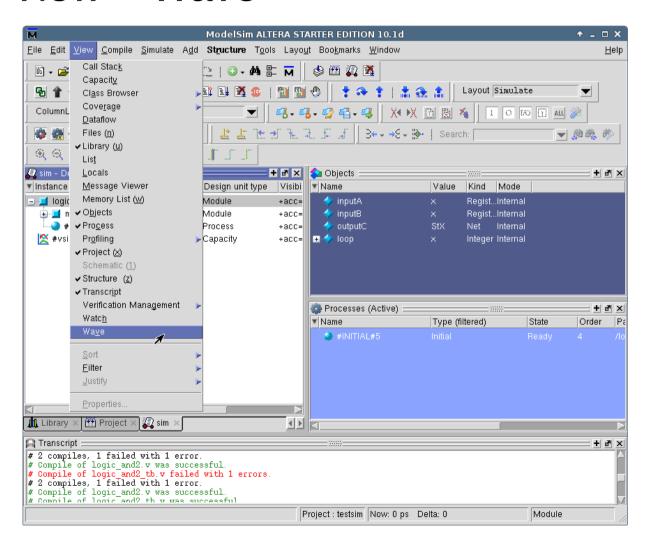
Simulating Design (cont.)

Once loaded you should see your module(s):



Menu: Waveform Viewer

Select 'View > Wave'





Waveform Viewer

 Appears as sub-window (on first run) ModelSim ALTERA STARTER EDITION 10.1d Wave viewer File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help window Layout Simulate 🗣 👚 🐃 🐃 | 👫 🛮 100 ps 🗦 🖺 🚉 🚉 📆 🤹 | ColumnLayout AllColumns I 0 1/0 [] ALL 🏄 3 - - - - Search: Q Q Q B + 🗗 × 🋺 sim - Default 🚾 Wave - Default 😑 🖎 Objects 🚐 + 3 × ▼ Instance Design unit Design Value Kind logic_and2_tb Moduli 🖃 🗾 logic_and2_tb Regist logic and2 Module 🔷 inputB Regis Select signal(s) #INITIAL#5 logic and2 tbProces outputC 🔀 #vsim capacitv# to view Processes (Active) + 3 X ▼ Name Type (filtered) #INITIAL#5 Now Library : 🏻 🛗 Project 🔀 🏭 sim 🗈 < > < Transcript + 3 × # 2 compiles, 1 failed with 1 error. # Compile of logic_and2.v was successful.
Compile of logic_and2_tb.v failed with 1 errors.
2 compiles, 1 failed with 1 error. # Compile of logic_and2.v was successful.
Commile of logic_and2 th v was successful

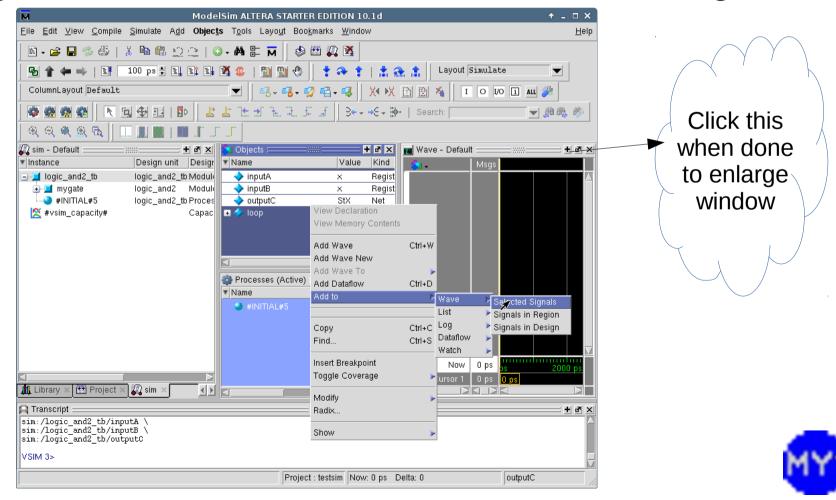
inputA

0 ps to 2480 ps

Project : testsim | Now: 0 ps | Delta: 0

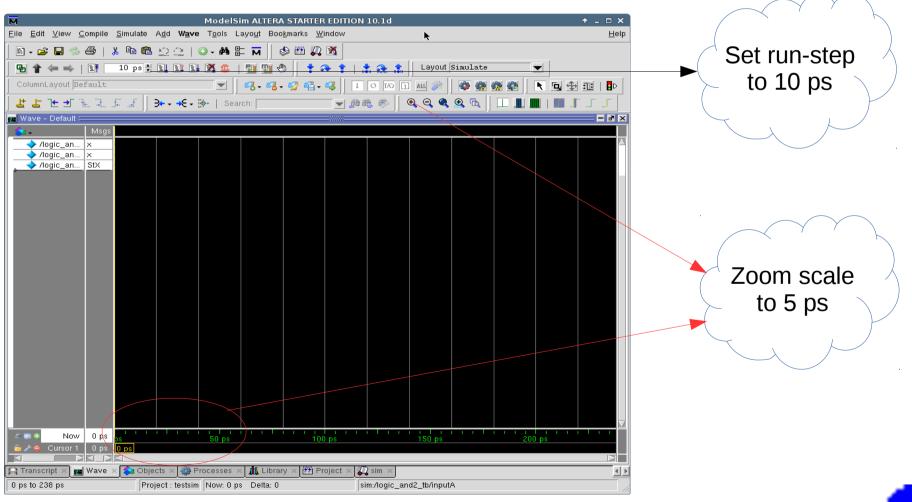
Wave Viewer: Adding Signals

- Select signals (Ctrl-click) inputA,inputB,outputC
 - Right-click, select 'Add to >Wave >Selected signals'



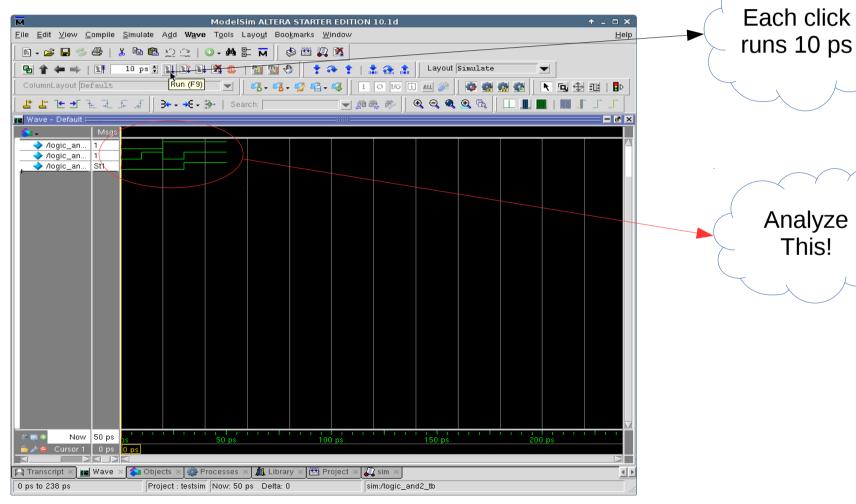
Ready to Execute (Simulation)

Change a few settings...



Executing/Running the Simulation

Click on Run (F9) icon...

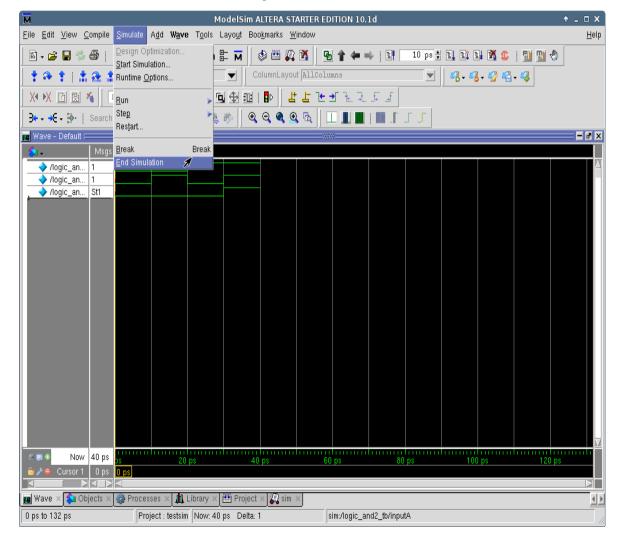




Running New Simulation

To run a new simulation, end the current

simulation





Practical Session 3.1

- Implement the given logic in truth table
 - You may choose to use 'assign' statements or 'always' block
- Create a suitable testbench for the modules
- Simulate and analyze the results to verify the functionality of the modules

iA	iB	iC	oD
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

