PGT302 – Embedded Software Technology

PART 4
Hardware Platform 2

Objectives for Part 4

- Need to DISCUSS and ANALYZE the following topics:
  - Board (GTUC51B001) specifications
    - startup sequence, bootloader
  - Microcontroller (8051) details
    - Features: I/O, Timer, Interrupt
  - Compare GTUC51B001 / P89V51RD2 against Raspberry Pi / BCM2835

GTUC51B001

- Basic Microcontroller Board
  - based on Intel 8051 core
- Used in Embedded Systems / Microcontroller courses
  - e.g. EKT322, PGT322 @UniMAP
  - classic usage in systems development
- Cost effective solution
  - still available in DIP package (easier to develop and maintain)
  - with high frequency variations, capable of solving many (if not most) practical applications

Platform Specifications

- GTUC51B001
  - NXP's P89V51RB2/RC2/RD2
  - FTDI FT232RL (USB-RS232 Converter)
  - IO with some specific functions (UART, SPI)
  - Powered using DC adapter OR USB (FTDI)
  - Optional extension board GTUC51X001
    - stackable, shared power lines
    - 16x2 Text LCD, 8-bit serial ADC, keypad interface
    - switches, LEDs

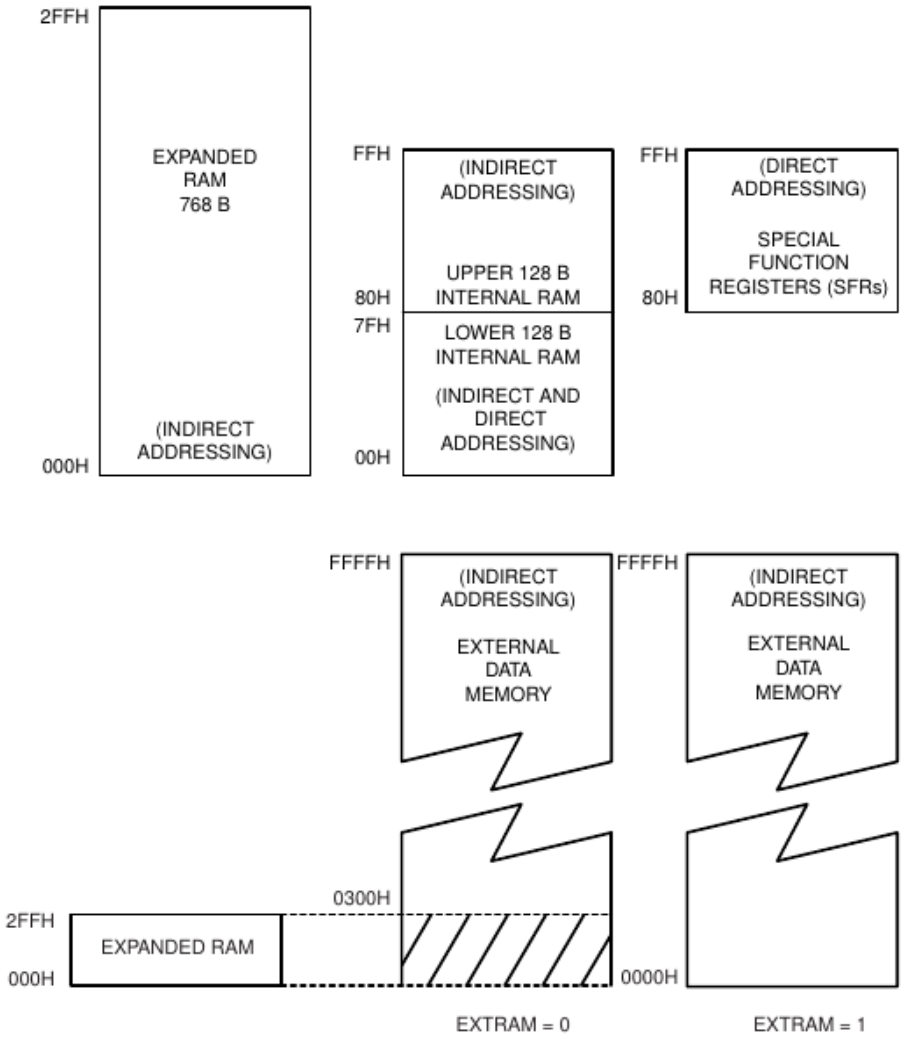
Startup sequence @bootstrap

- Like all 8051 cores, starts at address 0x0000
  - original 8051 has 4K EPROM
- P89V51 has flash memory at 0x0000
  - RB2/RC2/RD2 with 16/32/64kB blocks (Block 0)
  - separate 8kB boot block (Block 1)
  - send character 'U' to trigger Block 1
  - used set baud rate (auto-baud)
- On-chip bootloader
  - no need for separate programming board/circuit
  - uses Intel HEX format

Microcontroller Details

- P89V51RB2/RC2/RD2
  - 8-bit microcontroller based on 8051 core
  - 16/32/64kB flash user memory
  - 5V op. voltage, 0-40MHz op. frequency
  - X2 mode (6 clock per instruction, normal 12)
  - SPI, enhanced UART
  - Programmable Counter Array (PCA) with PWM and capture/compare functions
  - Programmable watchdog timer
  - Low power modes

P89V51 Address Map



P89V51 Memory Organization

- Internal 1kB RAM
  - lower 128B (00→7F) direct/indirect address
  - upper 128B (80→FF) indirect address ONLY
  - SFR (80→FF) direct address ONLY
  - expanded RAM (NXP feature) 768B (000-2FF) indirect address ONLY
    - using movx (declared as xdata in C)
    - clearing EXTRAM bit (SFR)
- Can still address external 64kB
  - not really needed for RD2 variant

P89V51 Registers

- General Purpose
  - 4 banks of 8x8-bit registers
  - lowest 32 bytes on-chip RAM
  - active bank access as R0-R7
  - the others can be accessed as RAM
- Special Function Registers
  - *refer next slide...*

30 – 7F	General Purpose Ram							
2F	7F	7E	7D	7C	7B	7A	79	78
2E	77	76	75	74	73	72	71	70
2D	6F	6E	6D	6C	6B	6A	69	68
2C	67	66	65	64	63	62	61	60
2B	5F	5E	5D	5C	5B	5A	59	58
2A	57	56	55	54	53	52	51	50
29	4F	4E	4D	4C	4B	4A	49	48
28	47	46	45	44	43	42	41	40
27	3F	3E	3D	3C	3B	3A	39	38
26	37	36	35	34	33	32	31	30
25	2F	2E	2D	2C	2B	2A	29	28
24	27	26	25	24	23	22	21	20
23	1F	1E	1D	1C	1B	1A	19	18
22	17	16	15	14	13	12	11	10
21	0F	0E	0D	0C	0B	0A	09	08
20	07	06	05	04	03	02	01	00
18 – 1F	Register Bank 3							
10 – 17	Register Bank 2							
08 – 0F	Register Bank 1							
00 – 07	Register Bank 0							

P89V51 Registers (cont.)

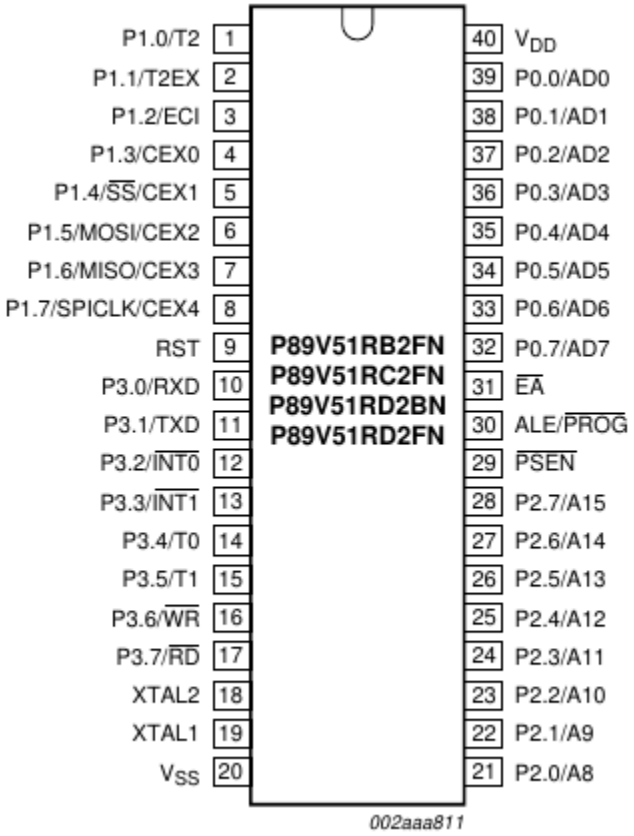
F8								FF
F0	**B**							F7
E8								EF
E0	**ACC**							E7
D8								DF
D0	**PSW**							D7
C8	**(T2CON)**		**(RCAP2L)**	**(RCAP2H)**	**(TL2)**	**(TH2)**		CF
C0								C7
B8	**IP**							BF
B0	**P3**							B7
A8	**IE**							AF
A0	**P2**							A7
98	**SCON**	**SBUF**						9F
90	**P1**							97
88	**TCON**	**TMOD**	**TL0**	**TL1**	**TH0**	**TH1**		8F
80	**P0**	**SP**	**DPL**	**DPH**			**PCON**	87

Bit/Byte addressable registers

Byte only addressable registers

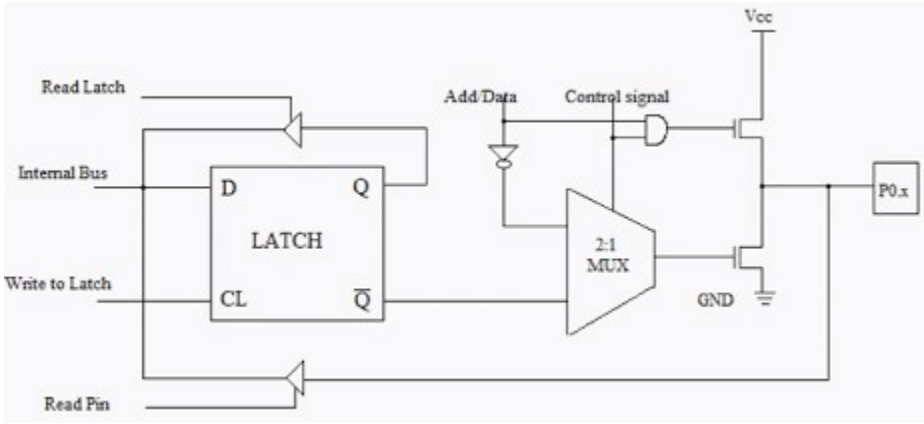
P89V51 40-pin DIP

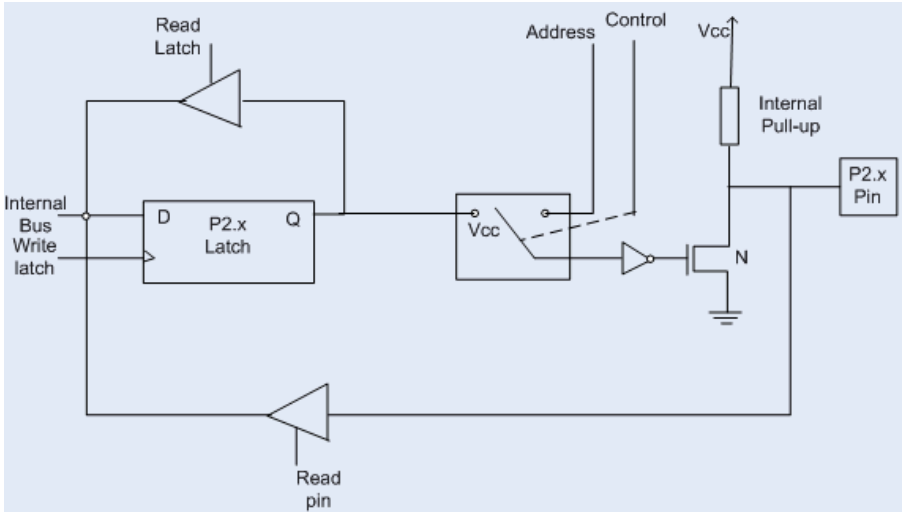
- 40-pin package
  - 32-pins (4 I/O ports)
  - 2-pin (V_{CC}/V_{SS})
  - ALE
  - EA (External Address)
  - XTAL1, XTAL2
  - PSEN (Read EXT code)
  - RST
- Some alternate functions
  - UART, SPI



P89V51 IO Pins

- 4x8-bits I/O Ports
  - 1 register per port
  - P0@80H, P1@90H, P2@A0H, P3@B0H
  - all pins have alternate functions
  - P0 open drain/collector
  - P1,P2,P3 has internal pull-ups





P89V51 Timer

- 2x16-bit timers/counters (T0, T1)
  - timer function triggers every machine cycle (i.e. for 6 clock machine cycle, 1/6 oscillator frequency)
  - counter function triggers with external input pins (T0 / T1)
  - each with 4 operating modes
    - mode 0: 13-bit timer with pre-scaler
    - mode 1: 16-bit timer/counter
    - mode 2: 8-bit auto-reload (TH reload value)
    - mode 3: single timer (T1 NOT used)
- 1x16-bit timer/counter (T2) (NXP feature)
  - 16-bit auto-reload, baud generator, etc.

P89V51 Timer (cont.)

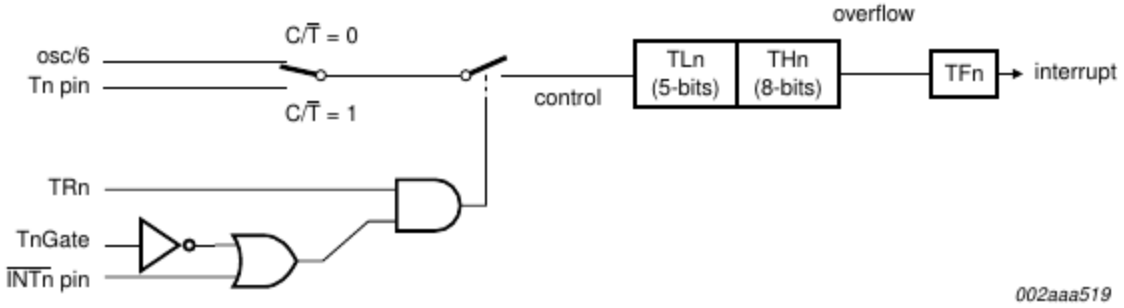


Fig 8. Timer/counter 0 or 1 in mode 0 (13-bit counter)

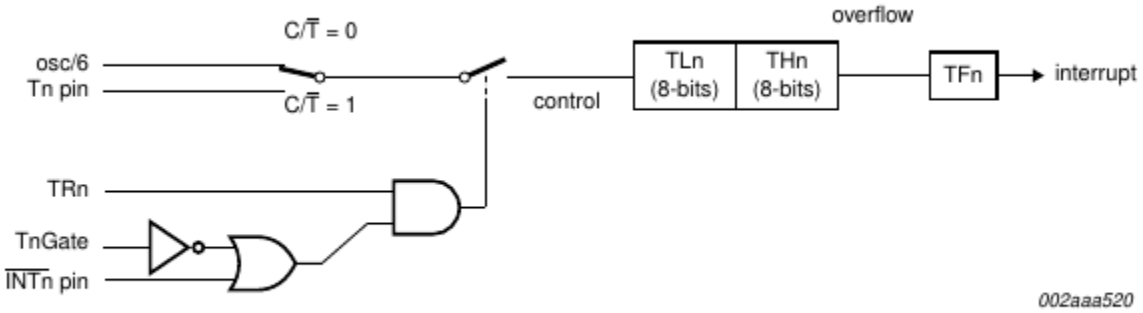


Fig 9. Timer/counter 0 or 1 in mode 1 (16-bit counter)

P89V51 Timer (cont.)

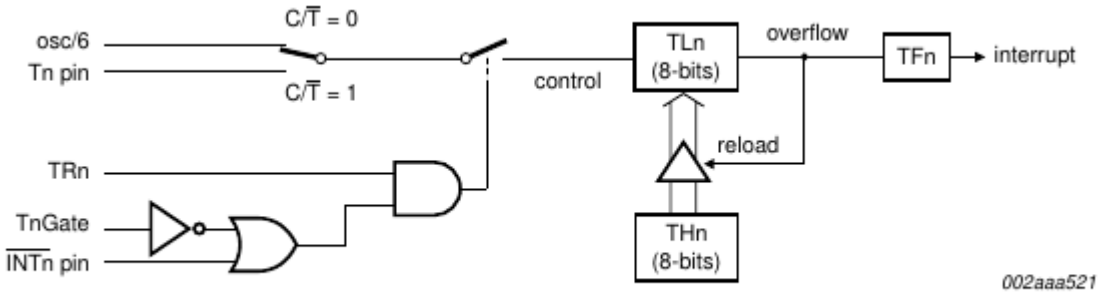


Fig 10. Timer/counter 0 or 1 in mode 2 (8-bit auto-reload)

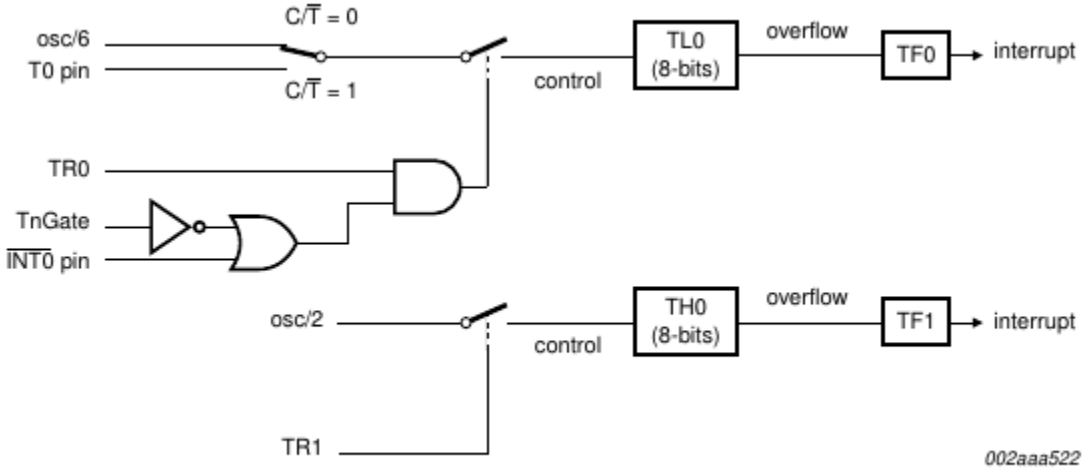


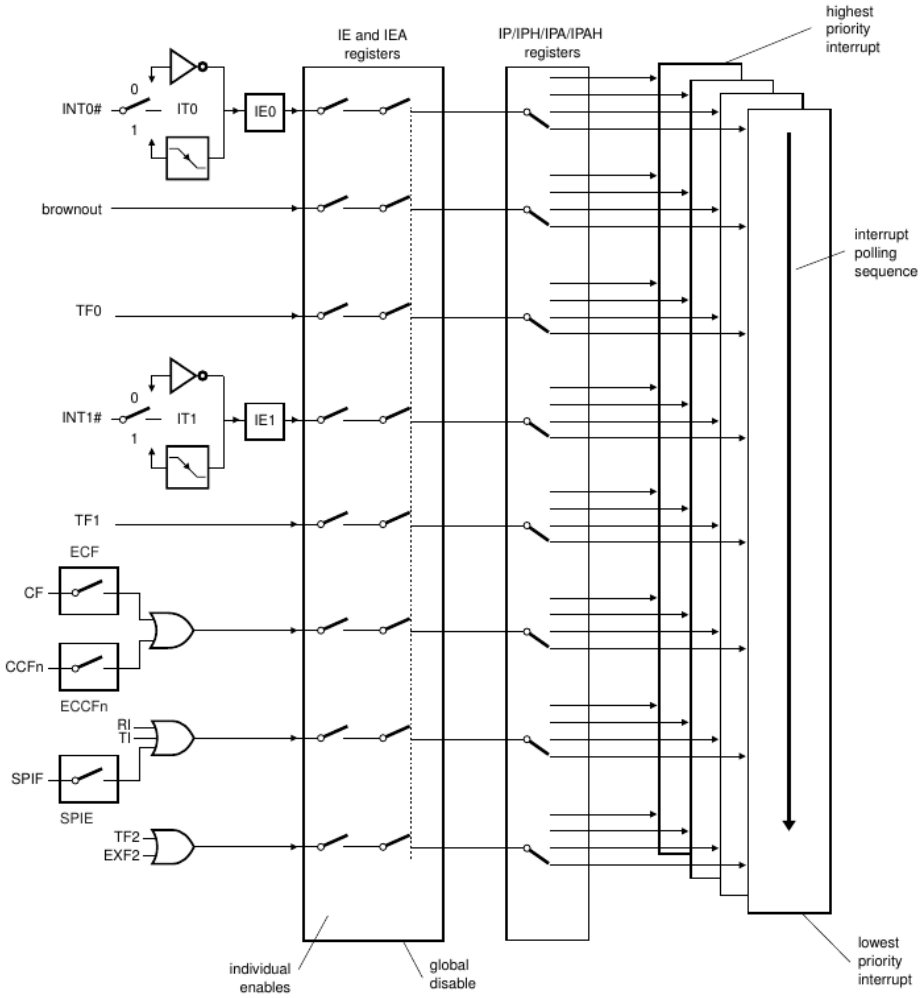
Fig 11. Timer/counter 0 mode 3 (two 8-bit counters)

P89V51 Interrupt

- 8 interrupt sources with 4 priority levels
  - 2 external interrupts (pins T0,T1)
  - 3 timer interrupts
  - 1 serial (SPI,UART) interrupt
  - PCA interrupt
  - Brownout (power supply fluctuation) interrupt

Description	Interrupt flag	Vector address	Interrupt enable	Interrupt priority	Service priority	Wake-up power-down
Ext. Int0	IE0	0003H	EX0	PX0/H	1 (highest)	yes
Brownout	-	004BH	EBO	PBO/H	2	no
T0	TF0	000BH	ET0	PT0/H	3	no
Ext. Int1	IE1	0013H	EX1	PX1/H	4	yes
T1	TF1	001BH	ET1	PT1/H	5	no
PCA	CF/CCFn	0033H	EC	PPCH	6	no
UART/SPI	TI/RI/SPIF	0023H	ES	PS/H	7	no
T2	TF2, EXF2	002BH	ET2	PT2/H	8	no

P89V51 Interrupt (cont.)



Platform Comparison

- Compare BCM2835 against P89V51RD2
  - general performance
  - I/O access
  - timer facility
  - interrupt facility
- Compare Raspberry Pi against GTUC51B001
  - programmability
  - I/O interfacing
  - display interfacing
  - application features

The End
of Part 4